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A HIGH RESOLUTION FASTER 64 BIT UT MULTIPLIER FOR DSP APPLICATIONS

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ABSTRACT:

Digital signal processors are the heart of audio processing, video processing and many other signal processing applications. FIR filter which uses the multiply and accumulate unit is the key component in the digital signal processor. The faster and the more precision of the multiplier in this FIR filter, the more will be the quality of the signal output. Several efforts are put to increase the fastness and precision of this multiplier. Urthava thiryakbhyam (UT) sutra of Vedic mathematics proved to be a short cut form of multiplication and proved to be faster. The UT multiplier, though faster, implemented with the conventional parallel multiplier is found to be somewhat slow. Also increasing the length of digital representation of the signal in terms of no of bits increases the precision. The recent processors are 32 bit and 64 bit processors. Booth multiplier is faster by reducing the partial product rows and as such, an attempt is made in this present work to implement 64 bit UT multipliers using booth multiplication for reducing partial products and it is found to be faster. An attempt is made in the present work to implement 64 bit Q-format multipliers using the Urthava thiryakbhyam principle with booth multiplication, which can be used with 64 bit processors. They are found to be faster in implementation. The present work is carried out in Xilinx ISE 12.1 targeted for porting into Spartan 6 FPGA. Experiments have been conducted on the present developed method and a number of the numerical analysis is made on the present method where there is an improvement in the performance based strategy followed by the entire system oriented outcome in a well accurate fashion respectively.

Keywords: Thirkabhyam urdhava, Mathematics of the Vedic strategy, Fixed point based fractional strategy.

1. INTRODUCTION

Author [9] developed the booth multiplier. Authors [7] implemented the Q-format multipler for digital signal processing applications. Authors [1] implemented the vedic multiplier with 16 and 32 bit in Q-format. In our present work a 64 bit Q-format multiplier for use with 64 bit processors that use UT multiplier with booth multiplication is implemented. The results have been analyzed along with the 16 and 32 bit UT multipliers also.

Urthava Thiryakbhyam sutra is from ancient Indian Vedic mathematics. These sutras were developed long back but written in Sanskrit were not popular until recently when they have been translated into other languages. The implementation of this mathematics combined with the signal processing applications proved to be very efficient and faster in VLSI implementation. As such there is an increasing trend towards utilization of these mathematical principles.

BLOCK DIAGRAM

The following block diagram shows the implementation of a 64 bit Q-format multiplier using Urdhava thiryakbhyam sutra. This multiplier has a regular structure on the silicon chip and as such is highly stable in working.

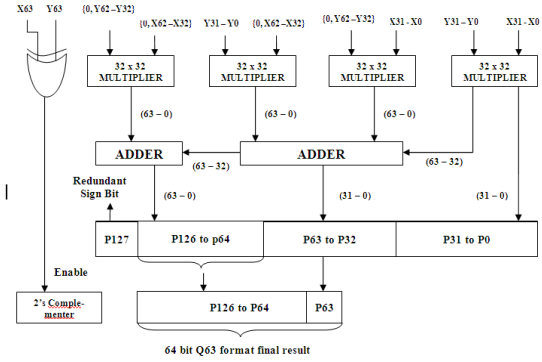

Fig 1: Shows the block diagram of the present method.

2. METHODOLOGY

In this paper a method is designed to keep the structure on the chip in a regular fashion. The 64 bit UT multiplier consists of four 32x32 multipliers and two adders. The output obtained is a 128 bit in which the least significant 64 bits are discarded to get the 64 bit final output, as the least significant bits in a fraction are of least importance.

The design is implemented in VHDL programming language in Xilinx ISE 12.1. The target device used for porting the design is Spartan 6 FPGA. Here the implementation of the present method is shown in the above figure in the form of block diagram. Here the present method completely overcomes the

drawbacks of the several previous methods sin a well oriented aspect respectively.

3. EXPECTED RESULTS

A lot of analysis is made on the present method and a huge number of the computations have been applied on the large number of the data sets in a well oriented fashion and it is applied related to the aspects of the different types of the environmental aspects respectively. Here the comparative analysis is made between the present method to that of the several previous methods and is shown in the below figure in the form of test bench representation and explains in the elaborative manner. Here the present method is effective and efficient in terms of the performance based strategy followed by the accurate outcome.

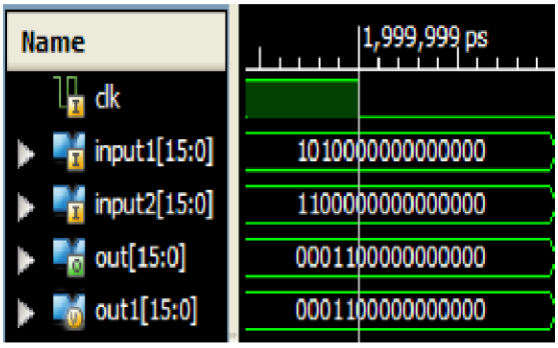

Fig 2: Shows the simulation results of Q-15 UT-multiplier

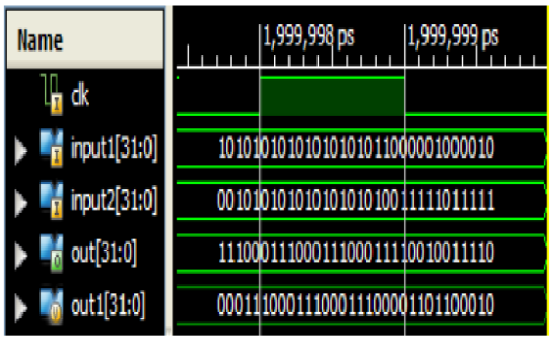

Fig 3: Shows the simulation results of Q-31 UT-multiplier

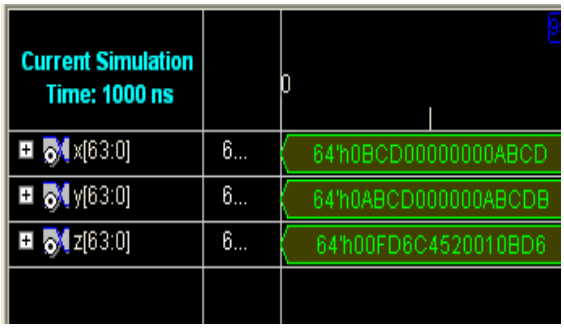

Fig 4: Shows the simulation results of Q-63 UT-multiplier

4. CONCLUSION

In this paper a method is designed for implementation of 64 bit q-format multiplier with for use with 64 bit processors, which is accurate in its implementation.. As the latest processors are of 64 bit this multiplier can be used in association with the latest processors. The next processors may come with 128 bit and as such there is the need to develop 128 faster multipliers for use with them.

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