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AN EFFICIENT ARCHITECTURE OF THE RADIX BASED FIR FILTER DESIGN

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ABSTRACT:

There is a huge popularity with rapid advancement in the technology related to the aspect of the implementation related to the number system oriented with respect to the binary based redundancy. FIR filter is the heart of the digital signal processor. The output of the FIR filter is got computed by the help of the response oriented strategy of the finite impulse based parameter in a well oriented fashion by the help of the operations related to the implementation aspects of the accumulation followed by the property of the multiplication respectively. Here a new technique is designed by a well effective framework oriented strategy where the implementation of the filter is carried out with the help of the computation related to the radix 256 orientation in a well effective strategy and the implementation of the arithmetic based on RB. Here, by the strategy of the encoding with the radix 256 booth's algorithm in a well oriented fashion, there is a total reduction in the complexity of the system followed by the aspect in the reduction of number of partial product rows by 8 fold. The RB addition is implemented to add the partial product rows without carry propagation which resulted in faster implementation. An improvement in the results has been observed. The performance is observed to be faster. Implementation of this FIR filter is carried out in XILINX ISE 12.1 ported into SPARTAN 6 FPGA. Experiments have been conducted on the present method and a number of analyses have been made where there is an accurate evaluation of the performance.

Keywords: Multiplier, Adder based strategy, Radix 256, computational complexity, Addition of the binary redundancy respectively.

1. INTRODUCTION

There is a rapid advancement in the system with respect to the communication oriented aspect. Authors of [2] to [5] implemented FIR filters with discrete coefficient values. Authors of [9] designed FIR filer in cascade form. Authors of [10] proposed CSHM algorithm for computation of FIR filter. Authors [1] implemented a 11 tap FIR filter. The present work is an FIR filter with 16 taps which has better response. The filter is implemented with Radix-256 booth encoding followed by RB addition. By this the complexity of the system is reduced to an effective level. Here the strategy is based on the realization based aspect related to the low power followed by the rapid speed. Filter related to the finite impulse related strategy plays a major efficient role for the implementation of the signal processing phenomena respectively.

BLOCK DIAGRAM.

Below are presented the general block diagram of FIR filter, block diagram of FIR filter with split sharing computation and the block diagram with radix-256 booth multiplier and RB addition for a 16 tap FIR filter.

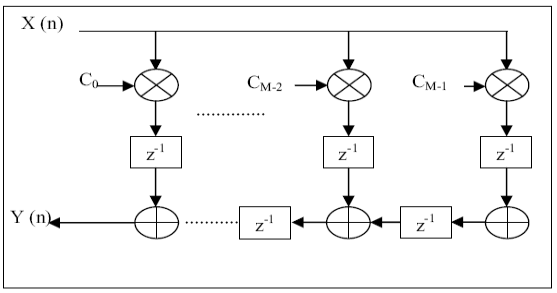

Fig 1: Shows the general implementation of FIR filter.

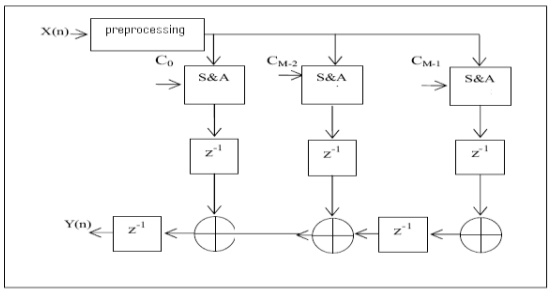

Fig 2: Shows the implementation FIR filter with split sharing multiplier (16 TAP)

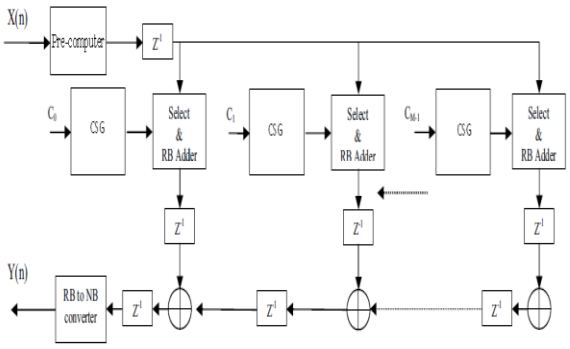

Fig 3: Shows the design structure with radix-256 booth encoding and RB addition for a 16 tap FIR filter.

2. METHODOLOGY

In this paper a method is designed with a well effective framework oriented strategy in a well effective manner where there is an improvement in the performance of the system followed by the accurate outcome. There is a huge challenge for the present method where it is supposed to accurately analyze the problems related to the several previous methods in a well effective manner followed by the accurate analysis of the theoretical aspect of the design oriented parameters of the present system.

In the present work the FIR filter is implemented in two methods and compared. In method 1, the split sharing multiplier, the input is preprocessed to get the odd multiples of input from 1X to 15X. The coefficient is divided into 4 parts and each part multiplied the input separately. The relative products are multiplied with the positional values and added to get the multiplier output. Every multiplication is carried out by suitably shifting the input. The products from various multiplied units are suitably delayed and added to get the filter output.

In the method 2, Radix-256 booth encoding with RB addition is carried out for a 16 tap FIR filter. The input is preprocessed to get the odd multiples from 1X to 15X. They are further processed to get the multiples from -128X to +128X. The select and add unit selects suitable two values out of them and converts to RB form. These two partial product rows are added to get the multiplier output in RB form. The multiplier outputs are suitably delayed and added to get the final filter output.

The results obtained in the two methods are compared and found that there is a substantial improvement in the performance of the filter implemented with Radix-256 booth encoding and RB addition as compared to the one with split sharing multiplier. Here the present method is effective and efficient in terms of the implementation based strategy as it does not involve any carry propagation for addition. Also there is no direct multiplication involved and multiplications are carried out by suitably shifting the input. This reduced the computational complexity and also the delay from input to output. We finally conclude that the present method completely overcome the problems related to the several previous methods and improve the performance of the system in an efficient manner. Here the implementation of the present technique is shown in the above figures in the form of the block diagrams or the circuit

connection representation and explains in a brief elaborative manner respectively.

3. EXPECTED RESULTS

A lot of analysis is made on the present designed method based on the finite impulse response of the radix-256 based strategy in a well effective manner followed by the huge number of the computations applied on the large number of the data sets. The delay performance is observed to have substantially improved. The simulation results obtained in both the methods are given below.

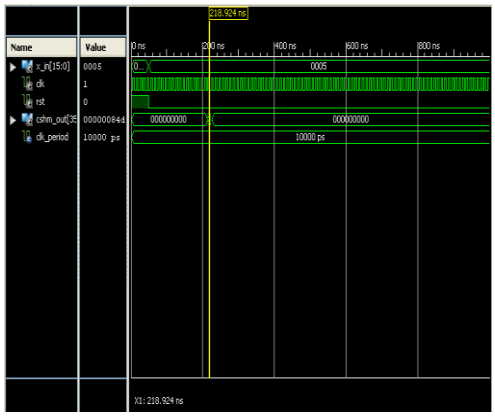

Fig 4: Simulation results of split sharing multiplier

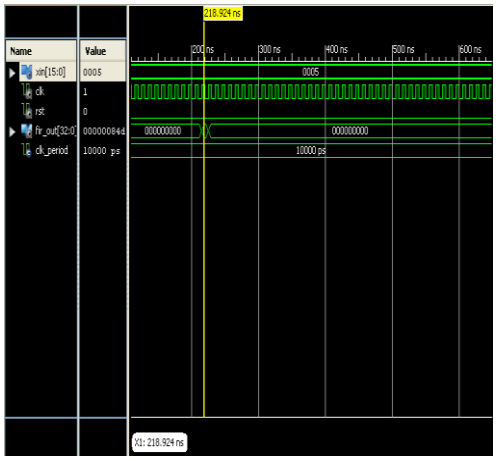

Fig 5: shows the simulation results of the present method implementation based strategy (1) For split sharing FIR filter and (2) for Radix-256 booth encoding with RB addition.

4. CONCLUSION

In this paper a 16 bit 16 tap FIR filter is implemented with Radix-256 booth encoding and RB addition, which has shown substantial improvement over the split sharing multiplier and the other methods. This has shown a very low delay from input to output and hence is highly useful for a practical implementation. This is the fastest method for implementation. We finally conclude that the design oriented parameters of the radix 256 plays a quite well effective role for the improvement in the performance based strategy followed by the accurate analysis.

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