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EFFECTIVE SYSTEM ARCHITECTURE BASED RISC STRATEGY

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ABSTRACT:

Embedded computers as well as personal computers have become the part and parcel of everyday human life. There is a rapid development in the computer structure. Several computers of different types are developed. Hence there is the deep need to introduce the architecture of the computer to everyone. Every engineer is supposed to know the best about computer. Also a strategy is now being developed to design the Intellectual Property core processors so that anyone could build his own computer/ embedded system as per his specific application. It is possible to build even reconfigurable processors so that the same processor can be reconfigured for different applications. Hence there is the deep need to develop the ability to build one's own processor to meet the needs of one's computing needs. This paper is such an attempt to introduce the RISC based design of processor for pedagogical purposes. This work introduces a processor that can perform all the general tasks such as addiction, subtraction, multiplication, division, AND, OR, XOR, NOT, load and store operations using logic based digital strategy. Embedded system design also becomes simple with the introduction of computer hardware for pedagogical purposes. Extensive testing has been carried out for testing the design and found to give accurate results. The processor is designed with Xilinx ISE 12.1 targeted for porting into the Spartan 6 FPGA kit. The design is quite synthesizable.

Keywords: Logic based on the digital strategy, Processor of the RISC fashion, CPU (central processing unit), Logic based programmable strategy respectively.

1. INTRODUCTION

Building a computer/processor from discrete components or ICs is a tough task. Any failure that occurs will cost a lot. Any modification required in between also may partially damage the system. Hence building computers for test/ teaching purposes require automation.

Author [8] made an approach to build computer with MSI components. Authors [6]-[7] designed simple computer using VHDL but lacked understanding of dataflow. Authors [2]-[5] made an approach that allowed interaction. Author [1] implemented RISC based processor with memory but not a full pledged one. Only addition, subtraction were introduced among arithmetic instructions and only AND, NOT and OR logic functions. In this paper a full pledged 8 bit RISC processor architecture is implemented along with RAM and ROM modules. The present design implements all the four arithmetic functions ADDITION, SUBTRACTION, MULTIPLICATION, DIVISION, and all the basic logical operations AND, OR, NOT and XOR operations. It also include load and store operations which are the very characteristic of RISC processors.

The design is implemented in VHDL in Xilinx ISE 12.1 targeted to Spartan 6 FPGA

BLOCK DIAGRAM

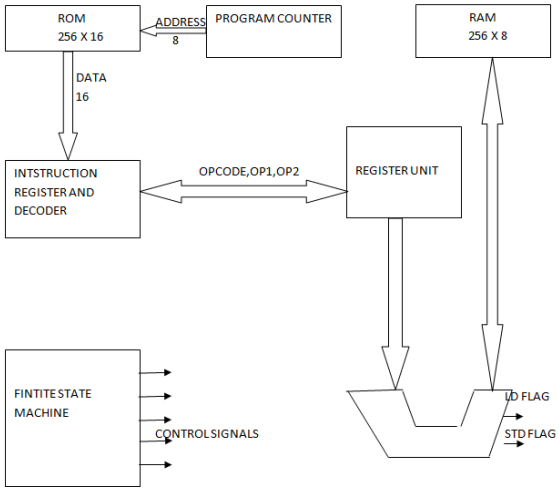

Fig 1: Shows the block diagram of the present method.

2. METHODOLOGY

There is a huge challenge for the present method where it is supposed to accurately analyze the problems of the several previous methods in a well efficient manner and also used for the theoretical aspect oriented analysis.

The present design is an 8 bit CPU and can execute 23 instructions. It is FSM based design which generates control signals. Instructions are 16 bit wide. Program memory is 16 bit wide. Data memory is 8 bit wide. It has 16 bit program bus and 8 bit program address bus. It has 8 bit data bus and 8 bit data address bus conforming to Harvard architecture.

Here the implementation aspect of the present method is shown in the above figure in the form of the block diagram and is explained in the elaborative fashion respectively. Here the present method completely overcomes the shortfalls of the several previous methods in a well efficient manner. Here we finally conclude that the present design oriented mechanism is effective and efficient in terms of the improvement in the system based aspect respectively.

3. EXPECTED RESULTS

A lot of analysis is made on the present method and the huge number of the simulations has been conducted on the large number of the data sets in a well oriented fashion respectively. A comparative analysis is made between the present method to that of the several previous methods is shown in the below figure in the form of the graphical representation and explains in a brief elaborative fashion respectively. There is a huge challenge for the present method where it is supposed to improve the performance of the system followed by the overall system based analysis with respect to the outcome of the entire system respectively. The present design is full pledged RISC processor. The simulation results showing the execution of all the instructions is shown in the figure below.

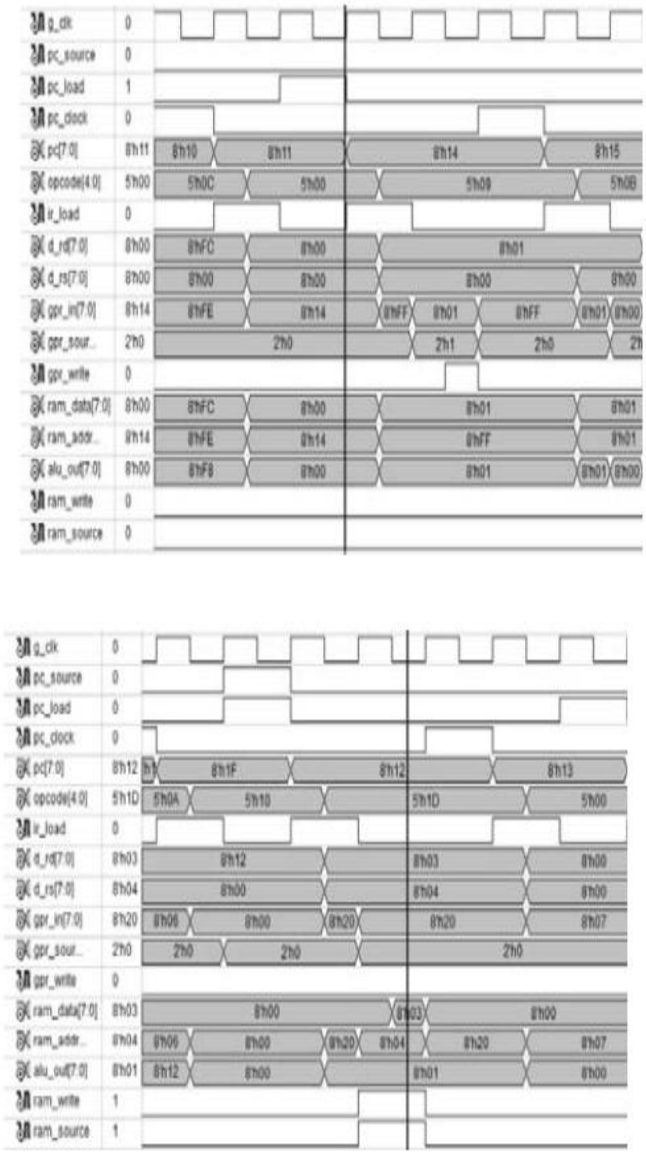

Fig 2: Shows the simulation results of the present implementation respectively

4. CONCLUSION

In this paper a method is designed with a particular framework oriented strategy to implement the RISC

architecture with all basic arithmetic and logical operations. It is used for the improvement in the performance in the system followed by the entire system based outcome. As the design is including all the basic functions of a processor and characteristics of the RISC processor, it is quite ideal for the educational purposes to explain the RISC processor. A lot of observation has been made depending on the platform oriented development based strategy followed by the design orientation of the specifications related to the aspect of the current strategy. Here we finally conclude that the present method is effective and efficient in terms of the performance based strategy followed by the accurate analysis with respect to the entire system based outcome in a well respective fashion respectively.

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