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SCHEMING OF HIGH SPEED LOW POWER CIRCUITS BY USAGE OF REVERSIBLE LOGIC

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ABSTRACT:

Reversible logic is extensively used within low power very-large-scale integration technology. Reversible circuits are able of back-computation as well as reduction in dissipated power, while there is no data loss. We utilize the proposal of reversible logic to break traditional speed-power trade-off, thus getting a step quicker to understand Quantum computing devices. Several combinational as well as sequential circuits are put into practice such as Ripple-carry Adder, Wallace Tree Multiplier, and Control Unit of GCD processor by means of Reversible gates. The power as well as speed parameters for circuits were compared by means of their traditional non-reversible counterparts.

Keywords: Reversible logic, Ripple-carry Adder, Wallace Tree Multiplier, Quantum computing devices, GCD processor, Back-computation.

1. INTRODUCTION:

Devices of quantum computing devices function at particularly high speed and consume infinitesimally low power. The basic reversible gates are in use to attain the necessary functionality of reversible circuit. Our work spotlights on functioning of reversible logic circuits in which most important intention is to optimize speed of design [1]. A Reversible adder is considered by means of basic reversible gates. By means of this adder, an 8-bit reversible ripple-carry adder is developed and afterwards compared with traditional

conventional 8-bit adder regarding speed, critical paths as well as hardware used. Then by means of same reversible adder, a Wallace tree multiplier was implemented, and compared with the traditional Wallace tree multiplier. As sequential circuits are heart of digital designing, design for control unit of a reversible GCD processor was proposed by means of Reversible logic gates. GCD processor incorporates a standard algorithm of Euclid that involves Subtract-Compare-Swap process of two numbers. In our work we utilize the proposal of reversible logic to break traditional speed-power trade-off, thus getting a step quicker to understand Quantum computing devices. To validate this research, a variety of combinational as well as sequential circuits are put into practice such as 4-bit Ripple-carry Adder, Wallace Tree Multiplier, and Control Unit of an8-bit GCD processor by means of Reversible gates [2]. The power as well as speed parameters for circuits were compared by means of their traditional non-reversible counterparts. The comparative statistical study confirms that circuits that employ Reversible logic thus are quicker as well as power efficient.

2. OVERVIEW OF REVERSIBLE LOGIC:

The design of reversible logic finds applications in a variety of fields. The individuality of reversible logic is that, there is no data loss as there is one-to-one correspondence among inputs as well as outputs which permits system to run backwards and at the same time doing so, any intermediate design stage is carefully examined. Boolean logic is considered as reversible when the set of inputs that are mapped contains an equivalent number of outputs mapped that is they contain one-to-one correspondence which is recognized by means of employing of reversible gates within designs. Any of the circuit that contains just reversible gates is able of dissolving no power. We utilize the proposal of reversible logic to break traditional speed-power trade-off, thus getting a step quicker to understand Quantum computing devices. The general goals of Reversible Logic are Quantum Cost: which is measure of functioning cost of quantum circuits. More exactly, quantum cost is described as number of elementary quantum operations necessary to comprehend a gate. Speed of Computation: The time delay of circuits has to be as low as feasible since there are

several computations that have to be performed within a system that involves a quantum processor; thus speed of computation is extremely significant parameter while investigating such systems. Garbage Outputs: These are those signals of output which do not contribute in driving of further blocks within the design. These outputs turn into redundant since they are not necessary for computation of later stage. The outputs of garbage make system slower; thus for better effectiveness it is essential to minimize number of garbage outputs. Feedback: Looping is severely prohibited when scheming of reversible circuits. Fan-out: The output of an assured block within design can simply drive at most single block within the design thus it can be said that Fan-out is limited to 1.

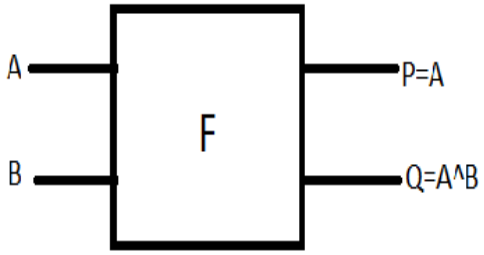

Fig. 1: Feynman Gate

3. AN OVERVIEW OF PROPOSED SYSTEM:

There are numerous reversible gates such as Feynman, Toffoli, and so on. As universal gates within boolean logic are Nand and Nor, in support of reversible logic, universal gates are Feynman as well as Toffoli gates. Feynman gate is common gate which is used in support of signal copying purpose or else to get hold of complement of input signal [3]. Toffoli gate is a common reversible gate which includes three inputs that are mapped towards three outputs. Our work spotlights on functioning of reversible logic circuits in which most important intention is to optimize speed of design. A Reversible adder is considered by basic reversible gates. By means of this adder, a reversible ripple-carry adder is developed and by means of same reversible adder, a Wallace tree multiplier was implemented, and compared with the traditional Wallace tree multiplier. In our work several combinational as well as sequential circuits are put into practice such as 4-bit Ripple-carry Adder, Wallace Tree Multiplier, and Control Unit of an8-bit GCD processor by means of Reversible gates. The power as well as speed parameters for circuits were compared by means of their traditional non-

reversible counterparts. The gate that is used in implementing a reversible ripple-carry full adder is TSG gate that functions like a complete adder. A reversible ripple-carry adder is quicker than non-reversible adder, since computation of carry within a reversible adder does not need computation of earlier stage carry. When earlier stage carry is forwarded within reversible adder, computation of earlier stage carry as well as computation regarding sum is completed at the same time while in irreversible adder subsequent stage carry cannot begin any computation till earlier stage carry is completely generated. A Wallace tree is a proficient hardwired functioning of digital circuit those multiply two integers. The Wallace tree includes three steps such as: each bit of multiplicand is multiplied by means of every bit of multiplier, hence providing n^2 results. Based on position of multiplied bits, wires carry various weights. The number of partial products is reduced to 2 by means of layers of full as well as half adders. The wires are clustered in two numbers, and added by means of a conventional adder. To show classical as well as reversible methods to Sequential Control Unit Design, reversible logic is in use for particular purpose processor that calculate GCD of two numbers. This processor incorporates a standard algorithm of Euclid that involves Subtract-Compare-Swap process of two numbers. The essential standard is to take away smaller of two numbers frequently from other number until we obtain the number that divide another. The design of reversible logic finds applications in a variety of fields that includes Quantum computing, Nano-computing, optical computing, Quantum Computing Automata which is a study of mathematical objects known as Abstract machines and computational problems that are solved by means of them, ultra- low power designing of VLSI, Quantum dot cellular and so on. The future of computer chips is restricted by means of Moore's law; thus an option is to put up quantum chips [4]. Our future research is scheming of a novel reversible gate as well as implementation reversible logic into absolute Quantum processor which is capable of ultra-high speed as well as infinitesimally low power computation.

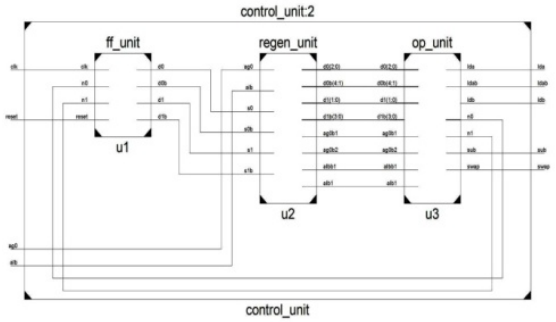

Fig2: GCD Control Unit

4. CONCLUSION:

Reversible logic was presented itself as a well-known expertise that plays an essential role within Quantum Computing. Our work spotlights on functioning of reversible logic circuits in which most important intention is to optimize speed of design. We make use of the proposal of reversible logic to break traditional speed-power trade-off, thus getting a step quicker to understand Quantum computing devices. To confirm this research, a variety of combinational as well as sequential circuits are put into practice by means of Reversible gates. The necessary standard is to take away smaller of two numbers frequently from other number until we obtain the number that divide another. The power as well as speed parameters for circuits were compared by means of their traditional non-reversible counterparts. The comparative statistical study confirms that circuits that employ Reversible logic thus are quicker as well as power efficient. The design of reversible logic finds applications in a variety of fields that includes Quantum computing, Nano-computing, optical computing, Quantum Computing Automata, ultra- low power designing of VLSI, Quantum dot cellular and so on.

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