IJRRECS/June 2016/Volume-4/Issue-6/5551-5558 **ISSN 2321-5461**

INTERNATIONAL JOURNAL OF REVIEWS ON RECENT ELECTRONICS AND COMPUTER SCIENCE

AN APPROACH TOWARDS INCREASE THE SUM OF INFLECTION INDICES & PROVIDES HIGHER ROTATING FORCE FOR A GIVEN INPUT DC-VOLTAGE

D.Subramanyam[1], B.Seshidher[2]

[1] *Assistant Professor, Dept. of Electrical and Electronics Engineering, St Mary's engineering college, Hyderabad, India*
214mani@gmail.com
[2]*Assistant Professor, Dept. of Electrical and Electronics Engineering, St Mary's Group of Institutions, Hyderabad, India*
seshi258@gmail.com

ABSTRACT:

A space vector modulation for nine-switch inverter is proposed as dual output inverter, this technique was compared with carrier based PWM technique and space vector modulation technique (SVM).The SVM technique increases the sum modulation indices up to 15% in contrast with conventional scheme, in which the sum of modulation indices is equal or less than 1. The additionally available high voltage for a given input dc-voltage translates to higher torque. And, we also presents a novel SVM technique with minimum-semiconductor switching and reduced THD, the cost of power devices, and thermal heat effect. This scheme will be advantages for high power applications, as the reduced THD method decreases total harmonic distortion. Finally, the performance of proposed SVM for nine-switch inverter is verified under simulation perfectly.

Keywords:-Nine–switch inverter, space vector modulation (SVM), minimum-semiconductor, THD method.

1. INTRODUCTION:

In many cases, there may be two or more ac loads that require independent control. The conventional solution is to use separate inverters which increases the volume and cost of the system. Hence,a dual output inverter has been proposed with nine-switch semiconductor, which is showed inFig. 1., and is used as ac-ac converter. The proposed nine-switch inverter is a combination of two conventional inverters with three common switches, in this sum of modulation index of two outputs must be less than or equal to 1. Therefore, voltage amplitude of outputs is smaller, compared with two separate inverters [4].This problem can be rectified by space vector modulation. In [1], carrier-based pulse width modulation (PWM) methods have been provided for nine-switch inverter. This paper proposes space vector modulation (SVM) methods for the aforementioned nine-switch inverter and also describes the carrier-based PWM control method for nine-switch inverter. Space Vector modulation (SVM) for nine-switch inverterincludes two special SVMs with minimum-semiconductor switches and reduced THD. These Techniques are verified through simulations practically.

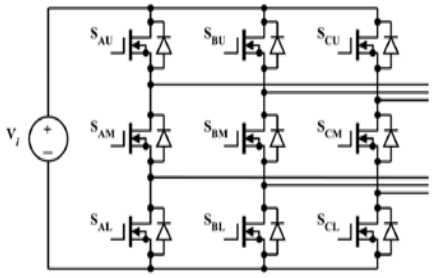


Fig.1. Nine-switch Inverter

II. CARRIER BASED PWM METHOD

The carrier-based PWM control method for nine-switch inverter is shown in Fig. 2. There are two reference signals (upper and lower) for each phase. These reference signals are related to upper and lower outputs respectively.

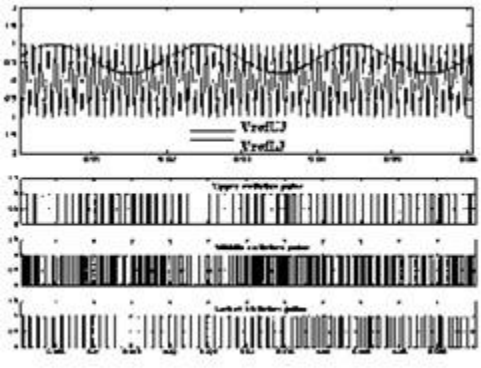


Fig.2. Carrier-based PWM method for nine-switch inverter

The gate signal for upper switch is generated by comparing the carrier signal and upper reference signal of the related phase (*Vref*UJ). Similarly, the gate signal for lower switch is generated from the carrier signal and lower reference signal of the related phase (*Vref*LJ). The gate signal

for mid switch is generated by the logical XOR of the gate signals for upper and lower switches. Inthis method, always two switches are ON in each leg. Carrier signal and upper reference signal of the related phase (*V*ref*UJ*). Similarly, the gate signal for lower switch is generated from the carrier signal and lower reference signal of the related phase (*V*ref*L J*). The gate signal for mid switch is generated by the logical XOR of the gate signals for upper and lower switches. With this method, always two switches are ON in each leg.

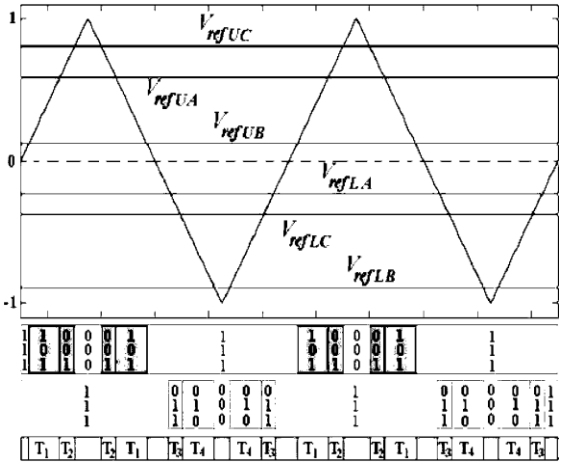


Fig.3. Carrier- based PWM method switching vector

Fig. 3 shows carrier-based PWM method switching vectors. There are six vectors in each switching cycle for both outputs: two nonzero vectors, one zero vector 0 0 0, two none zero vectors and one zero vector 1 1 1 *{*two active—short zero (0 0 0)—two active—long zero (1 1 1)*}*. In an active vector, output load is connected to the dc input source, when it is in zero vector, the output load is short-circuited.

III. SVM FOR NINE-SWITCH INVERTER

Each leg can be in three different semiconductors, ON-OFF position. These position can be called *{1}*, *{*0*}*, and *{2}*, as is illustrated in Table I. In Table I, *J* refers to leg *A*, *B*, or *C* and *U*, *M*, *L* refers to upper, mid, and lowersemiconductor respectively.

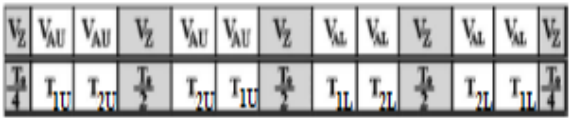


Fig.4 Typical SVM switching vector sequence

	S_{JU}	S_{JL}	S_{JM}
1	ON	OFF	ON
0	OFF	ON	ON
2	ON	ON	OFF

Table.1.Semiconductor On-Off Position of leg

Vector	Leg A	Leg B	Leg C	Type
1	1	0	0	Upper Active
2	1	1	0	
3	0	1	0	
4	0	1	1	
5	0	0	1	
6	1	0	1	
7	2	1	1	Lower Active
8	2	2	1	
9	1	2	1	
10	1	2	2	
11	2	1	2	
12				

13	1	1	1	Zero
14	0	0	0	
15	2	2	2	

Table.2.SVM Switching Vectors

The combination of switching vector of both outputs in Fig. 3 creates a specific sequence as shown in Fig. 4. This sequenceis used to design SVM method. There are 12 vectors in each switching cycle: *{*two upper active (V_{AU})—zero (V_Z)—two upper active (V_{AU})—zero (V_Z)—two lower active (V_{AL})—zero (V_Z)—two lower active (V_{AL})—zero (V_Z)*}*. The switching vectors are listed in Table.2. The vectors *V*1–*V*6 are upper active vectors. In these vectors, the upper output is in active state, and the lower output is in zero state. There is an inverse logic in lower active vectors (*V*7–*V*12). In zero vectors (*V*13–*V*15), both outputs are in zero state. Table.2 does not include all possible variations of switching states *{1}*, *{0}*, and *{2}*. Since a vector including *{2}* and *{0}* connects both loads to the dc source at the same time, the loads lose their individuality and they cannot have liberated frequencies. This is the intention for avoiding a vector that includes combinations of *{2}* and *{0}*. To determine the proper active vectors, two space vector diagrams are proposed as shown in Fig.5. The diagrams (a) and (b) are used to determine the upper and lower active vectors respectively. The SVM active vectors are determined with regard to the location of upper reference signal($\bar{v}refU$) in the diagram (a) and lower reference signal ($\bar{v}$refL) in the diagram (b). The reference signals for the upper and lower outputs are defined as:

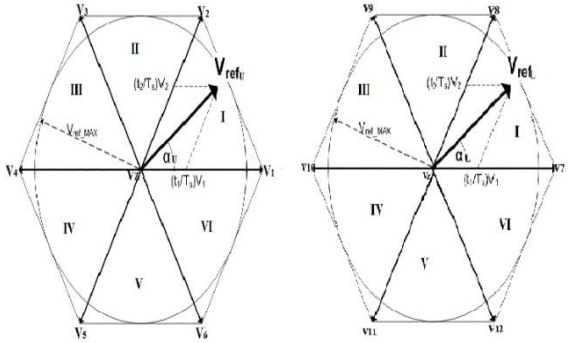
$$\bar{v}refU = VrefU\angle\alpha_U \quad (1)$$

$$\bar{v}refL = VrefL\angle\alpha_L \quad (2)$$

Where

$$\alpha_U = 2\pi f_U t + \emptyset_U \quad (3)$$

$$\alpha_L = 2\pi f_L t + \emptyset_L \quad (4)$$



Where,*fU*, *fL* are the frequencies, and $\emptyset_U$, $\emptyset_L$are the phases. All zero vectors *V*13, *V*14, and *V*15 can be used as zero states. The type of zero vectors can be selected based on control goals and optimizations such as minimum number of semiconductor switching

$$T_{1U} = \frac{\sqrt{3}}{2} m_U T \sin\left(\frac{\pi}{3} - \alpha_U\right) \quad (5)$$

$$T_{2U} = \frac{\sqrt{3}}{2} m_U T \sin(\alpha_U) \quad (6)$$

$$T_{1L}=\frac{\sqrt{3}}{2} m_L T \quad \sin\left(\frac{\pi}{3}-\alpha_L\right) \quad (7)$$

$$T_{2L}=\frac{\sqrt{3}}{2} m_L T \sin(\alpha_L) \quad (8)$$

$$To = T-T_{1U}-T_{2U}-T_{1L}-T_{2L} \quad (9)$$

Where,T_{1U},$T_{2U}$are the time interval of upper active vectors, T_{1L},$T_{2L}$are time of lower active vectors, *To* is time of zero vectors and *T* is switching period. $m_U$and mL are upper and lower modulation indices, respectively, and defined by

$$m_U=2\frac{VrefU}{Vi} \quad (10)$$

$$m_L=2\frac{VrefL}{Vi} \quad (11)$$

The sum of active vector time intervals must be less or equals to *T*. Thus, the following constrain must be satisfied .

$$(T_{1U}+T_{2U}+T_{1L}+T_{2L})\leq T \quad (12)$$

By substituting the values of T_{1U},T_{2U},T_{1L} andT_{2L}We get sum of modulation Indices as follows:

$$(m_U+m_L)\leq\frac{2}{\sqrt{3}}\approx 1.155 \quad (13)$$

Equation (12) clearly indicates that in the proposed SVM scheme, sum of modulation indices increases about 15% a very important feature to provide higher torque for a given input dc-voltage. For example, in case of washing machines, the above capability translates to higher machine capacity (in terms of cloth load) at high spin speed (e.g., 1800 r/min). A switching vector sequence for the proposed SVM is shown in Fig. 6. This switching sequence is developed to reduce the number of semiconductor switching. The zero vectors are placed between two upper and lower active vectors.

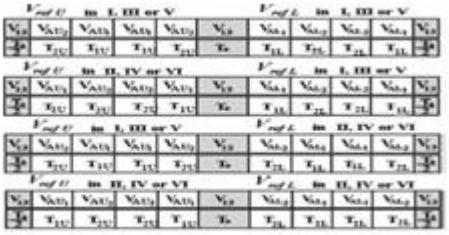


Fig.6. SVM with reduced number of semiconductor switching

In upper active vectors, legs are in state *{1}* or *{0}* and in lower active vectors, legs are in state *{1}* or*{−1}*. If *V*13 zero vector is placed between the active vectors, minimum number of switching is required. If*V*14 or *V*15 zero vectors are used then the number of switching is increased.There are two odd active vectors (*V*1, *V*3, *V*5, *V*8, *V*10, and *V*12) and two even active vectors (*V*2, *V*4, *V*6, *V*7, *V*9, and *V*11) in a switching sequence. In an even active vector, two legs are in state *{1}*, while in an odd active vector only one leg is in state *{1}*. If even active vectors are placed next to *V*13, number of switching will be reduced even more (see Fig. 6).

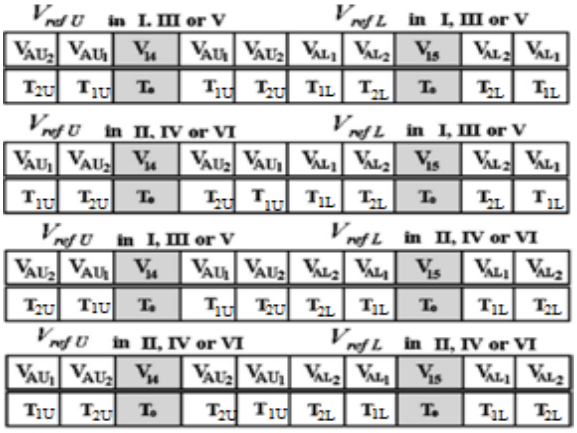


Fig.7. SVM with Reduced THD.

Also, there are other possible switch generation techniques such as switching method, to reduce THD. andto minimize THD. Active vectors for each output should be centrally placed within the switching period. Fig. 7 shows a switching vector sequence that shifts active vector into center of switching period, hence reducing THD. In this sequence, zero vectors are inserted between active vectors. In Fig. 7, *V*14 is inserted between upper active vectors and *V*15 is inserted between lower active vectors.

IV. SIMULATIONS AND EXPERIMENTAL RESULTS

Parameter	value
Switching frequency	3kH
f_U	25Hz
f_L	50Hz
R_{load}	20ohm
L_f	10mH
Nine switch inverter	m_U 0.50
	m_L 0.50

Table.3.Simulation Parameters

The proposed SVM are simulated for nine-switch inverter. Two Similar RL loads are connected to the outputs of inverter. Simulation parameters are listed in Table.3. Number of switching of semiconductors for nine-switch inverter and z-source-nine-switch inverter using carrier-based PWM and the proposed SVMs are shown in Table.4.

	SPWM	SVM(Minimum switching)	SVM(Minimum THD)
Nine-switch inverter	3500	2450	3400

Table.4.Number Of Semiconductor Switching

The nine-switch inverter with input dc source of 415V is simulated and implemented with reduced number of switching SVM. Figs. 8 and 9 show line-to-line voltage and phase voltage of both outputs, respectively

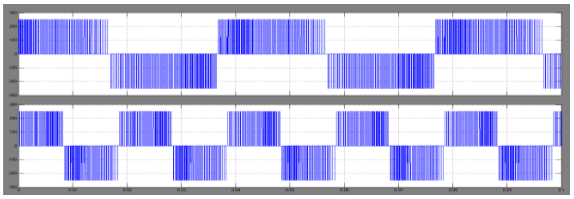


Fig. 8 Line voltage of Nine-switch inverter,(100 V/DIV, 10ms/DIV).

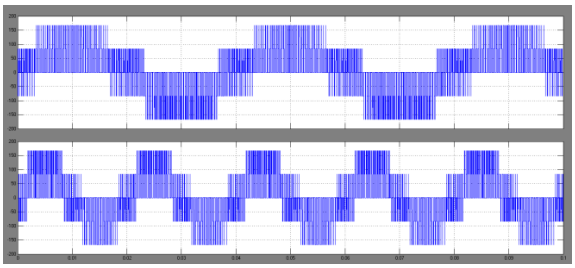


Fig.9. Phase voltage of Nine-switch inverter (min switching SVM), (100 V/DIV, 10ms/DIV).

It can be observed that the both outputs have expected frequencies. The load current is shown in Fig. 10. It can be seen that the load currents have nearly sinusoidal waveforms.

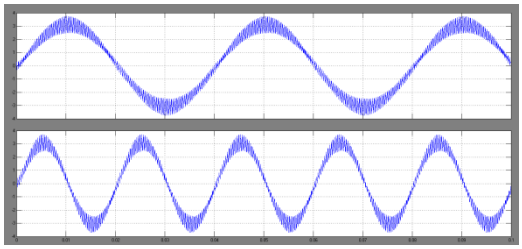


Fig.10.Output currents of Nine-switch inverter (min switching SVM). (10A/DIV, 10 ms/DIV)

Fig. 11 shows THD of load current versus load current magnitude for different cases: a) carrier-based PWM, b) reduced THD SVM and c) minimum semiconductor switching SVM

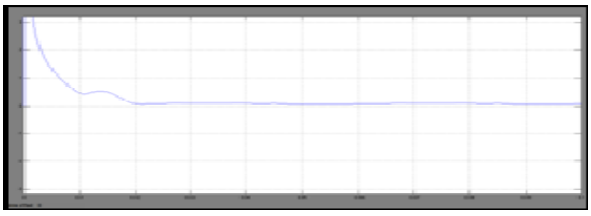


Fig .11(a). Carrier –based PWM method

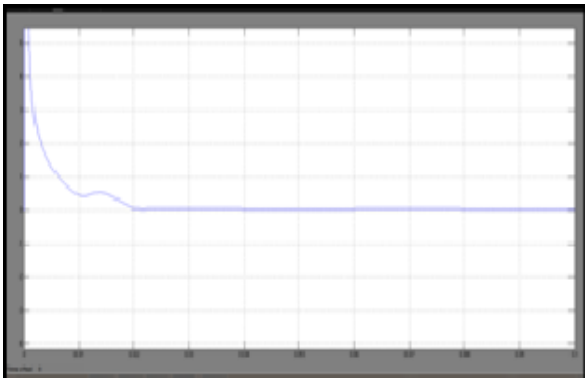


Fig .11(b). Reduced THD SVM method

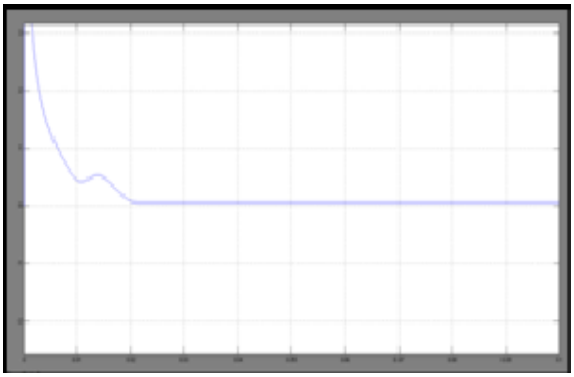


Fig.11(c) .Minimum semiconductor switching SVM

From the above simulation results THD for carrier–based PWM method is 7.6%, for minimum-semiconductor switching SVM method is 5.6%, and for reduced THD SVM method THD in load current is 4.7%.

V. CONCLUSION

In this paper, the proposed SVM nine-switch inverter, switching sequence is composed by the upper active vectors, the lower active vectors and the zero vectors.

The upper and lower active vectors are determined via two space vector diagram. The proposed SVM increases sum of modulation indices up to 15%, and it is an important feature in providing higher torque for a given input dc-voltage. The proposed SVM was simulated for the nine-switch inverter. The performance was verified using computer simulation. At the end, In future,this model has to be developed for nine switch- z-source inverter via extra shoot-through vectors.

VI. REFERENCES

[1] T. Kominami and Y. Fujimoto, "A novel nine-switch inverter for independent control of two three-phase loads," in Proc. IEEE Ind. Appl. Soc.Annu. Conf. (IAS), 2007, pp. 2346–2350.

[2] C. Liu, B. Wu, N. Zargari, and D. Xu, "A novel three-phase three-leg AC/AC converter using nine IGBTs," IEEE Trans. Power Electron., vol. 24, no. 5, pp. 1151–1160, May 2009.

[3] C. Liu, B.Wu, N. Zargari, andD.Xu, "A novel nine-switch PWM rectifierinverter\ topology for three-phase UPS applications," J. Eur. Power Electron.(EPE), vol. 19, no. 2, pp. 1–10, 2009.

[4] K. Oka, Y. Nozawa, R. Omata, K. Suzuki, A. Furuya, and K. Matsuse, "Characteristic comparison between five-leg inverter and nine-switch inverter," in Proc. Power Convers. Conf., Nagoya, 2007, pp. 279–283.