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SCHEMING OF AN EFFECTIVE SCHEME FOR MANAGING RAPID MULTIPLICATIONS

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ABSTRACT:

The techniques such as Vedic mathematics reduce time for processor so that it increases speed and moreover consider just few hardware elements. In Vedic maths calculation of complete partial products necessary for multiplication, are attained well in advance, much earlier than actual procedures of multiplication begin. Adders are most important blocks to complete the design of multiplier and the ripple carry adder is one of effortless adders which are constructed by means of cascading full adders blocks in series. Ripple adder is combination of four full adders where output carry is utilized as input carry to subsequent full adder. In our work we look at a new technique to improve the speed of Vedic mathematics multiplier by means of replacing traditional compressor based multipliers by ripple carry adder. The adder is recognized as a ripple-carry adder, as each carry bit ripples to subsequent full adder. The projected design contains reduced area, and increases speeds when compared to regular compressor based multiplier.

Keywords: Vedic mathematics, Ripple-carry adder, Compressor, Multiplier, Multiplication, Full adders.

1. INTRODUCTION:

Vedic word is obtained from the word Veda and it means knowledge storehouse. Vedic mathematics includes 16 sutras which it is related to various branches of mathematics such as algebra, arithmetic geometry. The major important highlights of method of Vedic maths is that calculation of entire partial products necessary for multiplication, are attained well in advance, much earlier than actual procedures of multiplication begin [1]. These partial products are afterwards added on the basis of Vedic maths algorithm to get hold of the concluding product and it leads to an extremely high speed method to carry out multiplication. Vedic Mathematics is divided into sixteen various sutras to carry out mathematical calculations and among these Urdhwa Tiryakbhyam chosen algorithms for performing multiplication. This word was originated from Sanskrit words meaning vertically as well as crosswise correspondingly. The most important benefit of utilizing this algorithm when compared to existing methods of multiplication is the fact that it make use of just logical AND operations, half adders as well as full adders to complete the operation of multiplication. Moreover the partial products necessary for multiplication are produced in parallel and earlier to real addition therefore saving most of processing time.

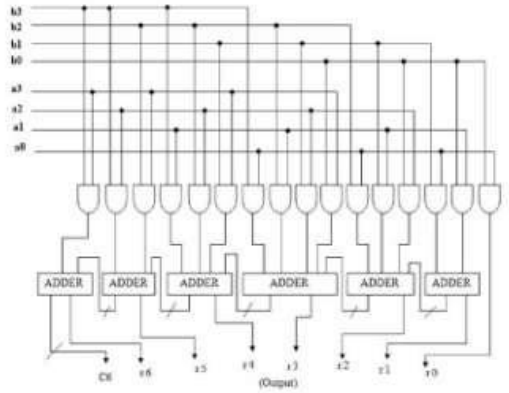

Fig.1: An overview of Urdhva Tiryakbhyam multiplier

2. METHODOLOGY:

The speed of any possessor relies on the performance of multiplier which leads to increase of demand for the multipliers of high speed, considering low area as well as reasonable power consumption. These multipliers are on the whole used in Digital Signal Processing, filtering as well as microprocessor applications [2][3]. The knowledge of Vedic mathematics is an extremely old and well-known method that serves as a foundation to solve quite a lot of mathematical challenges that are encountered in present day situation. Vedic Mathematics that is existed in ancient India was rediscovered and was bifurcated into sixteen simple sutras for performing of

mathematical calculations. For dealing with the drawbacks regarding speed of earlier methods, a new approach was introduced in the direction of multiplier design on the basis of ancient Vedic Mathematics. In our work we explore a new technique to improve the speed of Vedic mathematics multiplier by means of replacing traditional compressor based multipliers by Ripple Carry Adder. The ripple carry adder contains least area when measured to other adders hence it is restricted for applications where area have to be minimized, whereas speed is not significant. Ripple carry adder is considered by means of multiple full adders to include 8-bit numbers. The adder is known as a ripple-carry adder, as each carry bit ripples to subsequent full adder. The design of ripple-carry adder is easy, that permits for quick design time. Ripple adder is combination of four full adders where output carry is utilized as input carry to subsequent full adder. The benefits of Vedic math method is that calculation of the entire partial products necessary for multiplication, are gained well beforehand, earlier than actual multiplication begin. These products are later added on the basis of Vedic math‘s algorithm for obtaining of final product. This sequentially leads to extremely high speed method for performing multiplication. The proposed design contains reduced area, and increase speeds when compared to regular compressor based multiplier.

3. AN OVERVIEW OF PROPOSED SYSTEM:

The ease of Vedic mathematics sutras makes a way for its application in quite a lot of areas. The processor speed mainly depends on performance of multiplier which successively increase demand for multipliers of high speed, concurrently considering low area in addition to moderate power expenditure. With the start of novel technology within the fields of very-large-scale integration as well as communication, there is moreover an ever increasing demand for high speed processing as well as low area design. It is additionally a renowned piece of information that multiplier unit forms an important part of processor design [4]. Due to this, high speed multipliers turn out to be the requirement and in our work we introduce a novel means to enhance speed of a Vedic mathematics multiplier by means of replacing existing full adders as well as half adders of Vedic mathematics based multipliers. Vedic Mathematics that is existed in ancient India was rediscovered

and was bifurcated into sixteen simple sutras for performing of mathematical calculations. Adders are most important blocks to complete the design of multiplier. The Ripple Carry Adder contains the least area when measured to other adders hence it is restricted for applications where area have to be minimized, whereas speed is not significant. The ripple carry adder is one of effortless adders which are constructed by means of cascading full adders blocks in series. Ripple carry adder is considered by means of multiple full adders to include 8-bit numbers. The adder is known as a ripple-carry adder, as each carry bit ripples to subsequent full adder. One full adder is accountable for adding of two binary digits at any phase of ripple carry. The carryout of single stage is fed directly towards carry-in of next stage. Several full adders might be added to ripple carry adder or else ripple carry adders of various sizes might be cascaded to hold binary vector strings of outsized sizes. For parallel adder of n-bit, it needs n computational elements. A 4-bit ripple carry adder includes four full adders. The augends bits of m are added up to add end bits of n considerately of binary position. Each of the bit addition makes a sum as well as a carry out which is subsequently transmitted to carry in of subsequently higher-order bit. The 8x8 bit module of Vedic multiplier is simply implemented by means of using of four 4x4 bit modules of Vedic multiplier. By means of fundamental of Vedic multiplication, considering four bits simultaneously and by means of 4 bit multiplier block we can carry out the multiplication [5]. Outputs of 4x4 bit multipliers are added consequently to attain the concluding product. For performing of a comparison, several popular multipliers and additionally Ripple carry based Vedic multiplier were practised by Verilog as RTL language. When compared to area occupied by multiplier as well as its speed, with other popular multipliers, we can conclude that Ripple Carry based Vedic maths multiplier is an improved option over traditional multipliers used in quite a lot of complex circuits [6].

4. CONCLUSION:

There is an increase of demand for the multipliers of high speed, considering low area as well as reasonable power consumption. These multipliers are on whole used in Digital Signal Processing, filtering as well as microprocessor applications. The ease within Vedic

mathematics sutras makes a way for its application in quite a lot of well-known domains of engineering. Adders are most significant blocks to complete the design of multiplier. The Ripple Carry Adder contains the least area when measured to other adders hence it is restricted for applications where area have to be minimized, whereas speed is not significant. Quite a lot of full adders might be added to ripple carry adder or else ripple carry adders of various sizes might be cascaded to hold binary vector strings of outsized sizes. Here we explore a new technique to improve the speed of Vedic mathematics multiplier by means of replacing traditional compressor based multipliers by Ripple Carry Adder. The design of ripple-carry adder is simple, that permits for quick design time. Ripple adder is combination of four full adders where output carry is utilized as input carry to subsequent full adder. When compared to area occupied by multiplier as well as its speed, with other popular multipliers, proposed Ripple carry based Vedic maths multiplier is an improved option over traditional multipliers used in quite a lot of complex circuits.

REFERENCES

[1] Jagadguru Swami Sri Bharati Krisna Tirthaji Maharaja, ―VedicMathematics: Sixteen Simple Mathematical Formulae from the Veda,‖ pp. 5-45, Motilal Banarasidas Publishers, Delhi, 2009.

[2] Sushma R. Huddar, Sudhir Rao Rupanagudi, Kalpana M and Surabhi Mohan, ―Novel High Speed Vedic Mathematics Multiplier using Compressors‖, International Multi conference on Automation, Computing, Communication, Control and Compressed Sensing (iMac4s), 22-23March 2013, Kottayam, ISBN: 978-1-4673-5090-7/13, pp.465-469.

[3] Pushpalata Verma, K. K. Mehta" Implementation of an Efficient Multiplier Based on Vedic Mathematics Using EDA Tool" International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-1, Issue-5, June 2012

[4] Koren Israel,‖Computer Arithmetic Algorithms,‖ 2nd Ed, pp. 141-149, Universities Press, 2001.

[5] Hsiao, Shen-Fu, Ming-Roun Jiang, and Jia-Sien Yeh, "Design of high Speed low-power 3-2 counter and 4-2 compressor for fast multipliers, IEEE Electronics Letters, vol. 34, no.4, pp. 341-343, Feb. 1998.

[6] L. Ciminiera and A. Valenzano, "Low cost serial multipliers for high-speed Specialized processors, ―Computers and Digital Techniques, IEE Proc.E, vol. 135.5, 1988, pp. 259-265.