IJRRECS/November 2015/Volume-3/Issue-11/4870-4875 **ISSN 2321-5461**

INTERNATIONAL JOURNAL OF REVIEWS ON RECENT ELECTRONICS AND COMPUTER SCIENCE

TOWARDS A NOVEL DESIGNING OF QUATERNARY SIGNED DIGIT ADDER FOR IMPROVED PERFORMANCE

D.Niranjan Reddy[1], S.Mahaboob Basha[2]

[1]M.Tech Student, Dept of ECE, AVR & SVR Engineering College, Kurnool, A.P, India

[2]Assistant Professor, Dept of ECE, AVR & SVR Engineering College, Kurnool, A.P, India

ABSTRACT:

High performance adders are necessary as speed of digital processor will depend on adders speed and moreover serve as a unit for production of other operations. Speed of process is one of most important constraints in scheming of digital signal processor. We introduce quaternary signed digit number system for rapid and precise arithmetic operations. By practice of Quaternary signed digit numbering system it is likely to carry out carry free addition, multiplication, as well as borrow free subtraction. An Algorithm for scheming of quaternary signed digit numbering system adder is projected which is employed to write VHDL code for quaternary signed digit numbering system adders. Projected quaternary signed digit numbering system adder is improved than binary signed digit adders regarding number of gates, as well as delay although carry out addition in constant period. The system design has benefits of parallelisms in addition to decreased gate difficulty.

Keywords: Digital signal processor, Quaternary signed digit numbering system, Arithmetic operations, Adders, Radix system.

1. INTRODUCTION:

Most important challenge in the past for designing of VLSI design is to decrease area of chip by means of usage of effective methods of optimization. Later it has to increase the operation speed for attaining speedy calculations like, in the recent times, microprocessors millions of commands are

carried out for each second. In our work a quaternary signed digit numbering system was utilized for rapid and precise arithmetic operations [1]. In binary number system, computation speed is restricted by formation as well as transmission of carry particularly as number of bits enhances. By usage of Quaternary signed digit numbering system it is likely to carry out carry free addition, multiplication, as well as borrow free subtraction. This design is suitable for building of a high performance multiprocessor that consists of numerous processing elements. The benefit of carry free addition that is offered by quaternary signed digit numbering system numbers is utilized in scheming of speedy adder circuit. Adder that is designed with quaternary signed digit numbering system has a normal layout which is appropriate for VLSI functioning which is great benefit over Binary Signed Digit adders. An Algorithm for designing of quaternary signed digit numbering system adder is projected. This algorithm is employed to write VHDL code for Quaternary signed digit numbering system adders. A VHDL code in support of QSD adder is synthesized and timing report is made. The timing report provides delay time that is produced by adder structure. Carry free arithmetic process is implemented by means of a higher radix system for instance quaternary signed digit [2]. Carry free addition as well as borrow free subtraction is implemented for advanced number of bits by means of stable delay as well as less difficulty.

2. METHODOLOGY:

Binary signed-digit numbers will permit restricted carry propagation by means of difficult addition procedure that requires huge circuit for functioning. A unique higher radix-based illustration of binary signed-digit numbers will permit carry-free addition as well as borrow-free subtraction and offers other advantages for instance simplicity in logic as well as advanced storage density. Quaternary signed digit numbering system was utilized for rapid and precise arithmetic operations. By usage of quaternary signed digit numbering system it is likely to carry out carry free addition, multiplication, as well as borrow free subtraction. Proposed quaternary signed digit numbering system adder is improved than binary signed digit adders regarding number of gates, as well as delay although carry out addition in constant period. Projected design has benefits of parallelisms

in addition to decreased gate difficulty. The proposed digit numbering system will need a different prime modulo set that is based on logic elements in support of every arithmetic process. Carry free arithmetic process is implemented by means of a higher radix system. The computation speed as well as circuit difficulty will extend as number of computation steps decrease. A two step system will come into view to be a practical choice regarding computation speed as well as storage difficulty. The extent of redundancy will enhance with radix increase and signed digit system will permit us to put into practice parallel arithmetic by means of redundancy. In Quaternary signed digit numbering system carry propagation chain is removed that decrease computation time considerably, consequently improving of machine speed [3]. The proposed system is suitable for building of a high performance multiprocessor that consists of numerous processing elements. Quaternary signed digit numbering system will permit redundancy within number representations. The similar decimal number is recognized in more than one form of quaternary signed digit numbering system as a result we select such quaternary signed digit numbering system represented number that put off rippling of carry. The redundancy that is connected to signed-digit numbers will present option of carry free adding up [4]. Redundancy that is connected to signed-digit numbers will present fast addition as well as subtraction. Adding time for two redundant signed-digit numbers is continuous word length of operands, which is important towards high speed computation. In quaternary signed digit numbering system, each of the digits is described from -3 to 3. Carry free addition operations on huge number of digits are put into practice by means of continuous delay as well as less difficulty.

3. AN OVERVIEW OF PROPOSED SYSTEM:

Adders are usually used in a variety of electronic applications for instance processing of digital signal where adders will carry out different algorithms. Quaternary signed digit numbering system was utilized for rapid and precise arithmetic operations. This system is likely to carry out carry free addition, multiplication, as well as borrow free subtraction. The proposed quaternary signed digit numbering system will need a different prime modulo set that is based on logic elements in support of every

arithmetic process. Carry free arithmetic process is implemented by means of a higher radix system for instance quaternary signed digit. This design is suitable for building of a high performance multiprocessor that consists of numerous processing elements and it will permit redundancy within number representations. Proposed digit numbering system adder is improved than binary signed digit adders regarding number of gates, as well as delay although carry out addition in constant period and the projected design has benefits of parallelisms in addition to decreased gate difficulty. In the proposed quaternary signed digit numbering system carry propagation chain is removed that decrease computation time considerably, consequently improving of machine speed. As range of quaternary signed digit numbering system is from -3 to 3 and decimal numbers within range of -3 to +3 is denoted by one digit quaternary signed digit numbering system. As decimal number will go on from this range, more than single digit of quaternary signed digit numbering system is necessary [5]. Addition of two quaternary signed digit numbering system is made in two stages such as in the first stage of adder produce intermediate carry as well as intermediate sum from input digits. In the second stage of adder will add intermediary sum of present digit by intermediary carry of lesser important digit. There are two stages that are involved in carry-free addition and the initial step will construct an intermediate carry as well as sum from addend. The second phase will merge intermediary sum of current digit by carry of lesser important digit. To put off carry from rippling, two rules are defined such as initial rule will state that magnitude of intermediate sum have to be less than or else equivalent to 2. The second rule will describe that extent of carry have to be less than or else equivalent to 1 as a result, extent of second phase output is not more than 3 that is represented by single-digit quaternary signed digit numbering system; thus no carry is necessary. In the initial step, the entire promising input pairs of addend are measured [6]. Quaternary signed digit numbering system will hold two stages for adding up. The first stage will produce intermediary carry as well as sum in relation to the defined. In second stage intermediate carry from lesser important digit is combined towards intermediary sum of present digit that outcomes in carry free output.

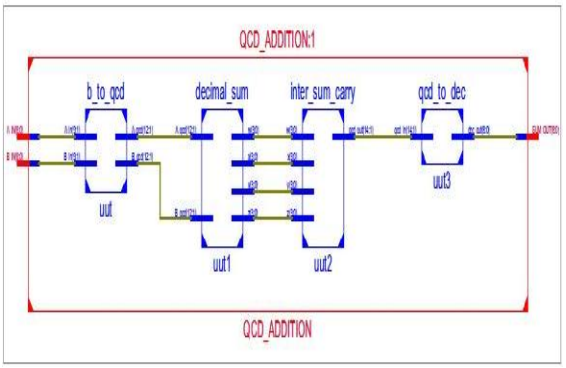

Fig1: RTL Schematic for 8-bit QCD addition

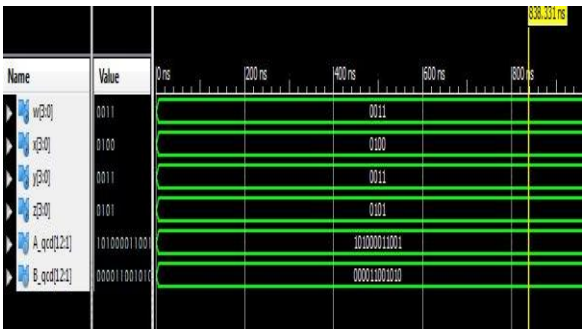

Fig2: simulation result for addition of QCD format

4. CONCLUSION:

With binary number system, computation speed is restricted by means of propagation of carry as number of bits improves. In our work we introduce a quaternary signed digit number system for rapid and precise arithmetic operations. Carry free arithmetic process is put into practice by means of a higher radix system for instance quaternary signed digit. By using of quaternary signed digit numbering system it is likely to carry out carry free addition, multiplication, as well as borrow free subtraction. An Algorithm for designing of quaternary signed digit numbering system adder is projected. The timing report will offer delay time that is produced by adder structure. Projected quaternary signed digit numbering system adder is superior than binary signed digit adders regarding number of gates, as well as delay although carry out addition in constant period. Adder that is considered with quaternary signed digit numbering system has a normal layout which is appropriate which is great benefit over binary signed digit adders. Projected design has profits of parallelisms in addition to decreased gate difficulty. Quaternary signed digit numbering system will allow redundancy within number representations.

REFERENCES

[1] Behrooz perhami "generalized signed digit number systems, a unifying frame work for redundant number reperesentation ".IEEE transactions on computers,vol 39,no.1,pp.89-98,January 1990.

[2] O. Ishizuka, A. Ohta, K. Tannno, Z. Tang, D. Handoko, "VLSI design of a quaternary multiplier with direct generation of partial products," Proceedings of the 27th International Symposium on Multiple-Valued Logic, pp. 169-174, 1997.

[3] A.A.S Awwal, Syed M. Munir, A.T.M. Shafiqul Khalid, Howard E. Michel and O. N. Garcia,

"Multivalued Optical Parallel Computation Using An Optical Programmable Logic Array", Informatica, vol. 24, No. 4, pp. 467-473, 2000.

[4] Kai Hwang, "Computer Arithmetic Principles, Architecture and Design", ISBN 0-471-03496-7, John Wiley & Sons, 1979.

[5] P. K. Dakhole, D.G. Wakde, " Multi Digit Quaternary adder on Programmable Device : Design and verification", International Conference on Electronic Design, pp. 1-4, Dec 2008.

[6] Behrooz Parhami, "Carry-Free Addition of Recoded Binary Signed- Digit Numbers", IEEE Transactions on Computers, Vol. 37, No. 11, pp. 1470-1476, November 1988.