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POWER DISSIPATION REDUCTION OF LOGIC CIRCUITS USING MTCMOS METHOD

Ch.Srikanth Reddy[1], A.Mohan[2]

[1]M.Tech(DSCE), Dept of ECE, GNITC (Gurunanak Institutions Technical Campus), Hyderabad, A.P, India
csri-reddy@yahoo.com
[2]Professor, Dept of ECE, GNITC (Gurunanak Institutions Technical Campus), Hyderabad, A.P, India
ashwala@yahoo.com

ABSTRACT:

As technology scales into the metric linear unit regime ground bounce noise and noise immunity are getting vital metric of comparable importance to run current, active power, delay and space for the analysis and style of advanced arithmetic logic circuits. During this paper, low run 1bit full adder cells are projected for mobile applications with low ground bounce noise and a unique technique has been introduced with improved staggered part damping technique for any reduction within the peak of ground bounce noise. Noise immunity has been fastidiously thought-about since the numerous threshold current of the low threshold voltage transition becomes a lot of vulnerable to noise. we tend to introduced a brand new semiconductor device electronictransistor semiconductordevice semiconductorunit semiconductor} resizing approach for 1bit full adder cells to work out the optimum sleep transistor size that scale back the run power and ground bounce noise. The simulation results depicts that the projected style additionally ends up in economical 1bit full adder cells in terms of standby run power, active power, ground bounce noise and noise margin. We've performed simulations victimization DSCH and Export small Wind normal CMOS technology at temperature with offer voltage of 1.2V.

Keywords:- Low leakage power; Noise Margin; Ground bounce noise; Optimal Sleep transistor and Adder cell.

1. INTRODUCTION:

Adder's area unit heart of process circuits and plenty of complicated arithmetic circuits area unit supported the addition [1], [2]. The large use of this operation in arithmetic functions attracts lots of researcher's attention to adder for mobile applications. In recent years, many variants of various logic designs are planned to implement 1-bit adder cells. These adder cells normally aimed to scale back power consumption and increase speed. These studies have conjointly investigated totally different approaches realizing adders victimization CMOS technology [3],[4]. For mobile applications, designers ought to work inside a really tight escape power specification so as to satisfy product battery life and package price objectives. The designer's concern for the extent of escape current isn't associated with making certain correct circuit operation, but is related to minimize power

dissipation. For transportable electronic devices this equates to maximising battery life. as an example, mobile phones have to be compelled to be supercharged for extended periods (known as standby mode, throughout that the phone is in a position to receive Associate in Nursing incoming call), however area unit absolutely active for a lot of shorter periods (known as speak or active mode, whereas creating a call). Once Associate in nursing device like a movable is in standby mode, bound parts of the electronic equipment inside the device, that area unit active once the phone is in speak mode, area unit close up. These circuits, however, still have escape currents running through them, even supposing they need been de-activated. Though the escape current is far smaller than the conventional operative current of the circuit. The escape current depletes the battery charge over the comparatively long standby time, whereas the operative current throughout speak time solely depletes the battery charge over the comparatively short speak time. As a result, the escape current contains a disproportionate impact on total battery life. this can be why building low escape adder cells for mobile applications area unit of nice interest. To summarize, some performance criteria area unit thought of within the style and analysis of adder cells, like escape power, active power, ground bounce noise, area, noise margin and lustiness with reference to voltage and electronic transistor scaling yet as variable method and compatibility with close circuitries. Shortening the gate length of a electronic transistor will increase its power consumption as a result of the enlarged escape current between the transistors supply and drain once no signal voltage is applied at the gate [5], [6]. Additionally to the sub threshold escape current, gate tunneling current conjointly will increase as a result of the scaling of gate chemical compound thickness. every new technology generations results nearly a 30xincrease in gate escape [7], [8]. The escape power is anticipated to achieve quite five hundredth of total power in sub 100nm technology generation [9]. Hence, it's become extraordinarily vital to develop style techniques to scale back static power dissipation in periods of inactivity. the facility reduction should be achieved while not trading- off performance that makes it tougher to scale back escape throughout traditional (runtime) operation. On the opposite hand, there area unit many techniques to scale back escape power [10].Power gating is one such standard technique wherever a sleep electronic transistor is side between actual ground rail AND circuit ground (called virtual ground) [11], [12], [13], [14]. This device is turned off within the sleep mode to cut-off the escape path. it's beenshown that this system provides a considerable reduction in escape at a negligible impact on performance [15], [16] , [17], [18] and any peak of ground bounce noise is feasible with planned noveltechnique with improved staggered section damping techniqueThis paper focuses on reducing sub threshold escape power consumption and ground bounce noise.The remainder of this paper is organized as follows. In section II, planned nano- CMOS full adder circuits, and its equivalent circuits area unit mentioned. In section III, the performance analysis and simulation results of typical CMOS full adder cell and planned circuits area unit explained. Then the paper is summarized in section IV.

II. PROPOSED FULL ADDER CIRCUITS

Recently, power dissipation has become a vital concern and goodly stress is placed on understanding the sources of power and approaches to managing power dissipation [3].Static logic vogue offers strength against noise effects, therefore mechanically provides a reliable operation. Pseudo NMOS and Pass-transistor logic will cut back the quantity of transistors needed to implement a given logic operate. however those suffer from static power dissipation. Implementing Multiplexers and XOR primarily based circuitsar advantageous once we implement by the pass semiconductor logic [4]. On the opposite hand, dynamic logic implementation of complicated operate needs alittle atomic number 14 space however charge leak and charge refreshing ar needed that reduces the frequency of operation. In general, none of the mentioned designs will contend with CMOS vogue in strength and stability [4], [13].Fig. one shows the standard CMOS twenty eight semiconductor adder [12]. this is often thought of as a Base case throughout this paper. All comparisons ar finished Base case.The CMOS structure combines PMOS pull up and NMOS pull down networks to supply thought of outputs.Transistor sizes ar mere as a magnitude relation of Width/Length (W/L). The filler of transistors plays a key role in static CMOS vogue. it's discovered within the typical adder circuit that the semiconductor magnitude relation of PMOS to NMOS is two for Associate in Nursing electrical converter and remaining blocks additionally followed a similar ratios once we thought of the remaining blocks as the same inverters. This magnitude relation doesn't provide best results with relation to noise margin and standby leak power once it's simulated in 90nm method. changed adder circuits with filler ar projected in Design1 and Design2 targeting the noise margin, and ground

bounce noise. Further, power gating technique is employed to cut back the leak power, wherever a sleep semiconductor is connected between actual ground rail gate ground. Ground bounce noise is being calculable once the circuits are connected with a sleep semiconductor. Further, the height of ground bounce noise is achieved with a projected novel technique. Modifiedsizing'sare shown in Fig. 2 and Fig. five severally. the littlest semiconductor thought of for 90nm technology incorporates a breadth of one20nm and a length of 100nm and offers W/L magnitude relation of 1.2. The W/L magnitude relation of NMOS is mounted at one.2 and W/L of PMOS is three.8 which is 3.1 times that of NMOS in Design1. The sizing of each block is based on the following assumption.

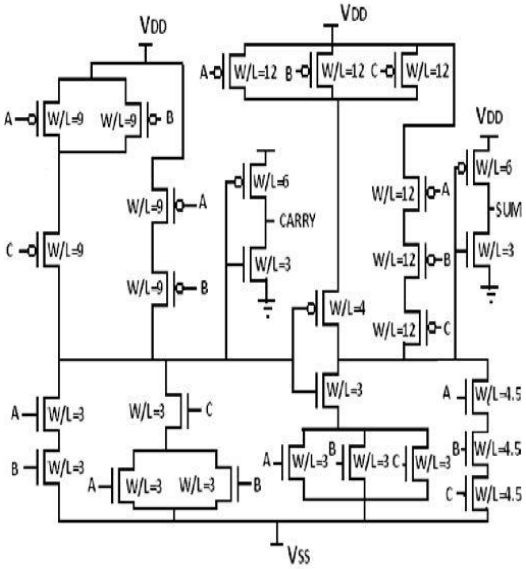

Figure 1. Conventional CMOS full adder.

Base case is taken into account as individual block as shown in Fig. 3. every block has been treated as identical electrical converter. identical electrical converter quantitative relation is maintained on every block. These filler can scale back the standby run current greatly as a result of sub threshold current is directly proportional to the Width/Length quantitative relation of junction transistor. On the opposite hand, these scale back sizes can reduce the world occupied by the circuit. this may scale back the semiconductor device space and clearly there'll be a discount within the value.Modified adder circuit i.e Design2 shown in Fig. 5, the W/L quantitative relation of PMOS is one.5 times that of W/L quantitative relation of NMOS and every block has been treated as identical electrical converter. Identical electrical converter size has been maintained on every block as shown within the Fig. 4. The goal of this style is to scale back the standby run power. Any compared to the bottom case and Design1 and ground bounce noise created once a circuit is connected to sleep junction transistor. However, there'll be a small variation on the noise margin levels and is nearly capable the bottom case.

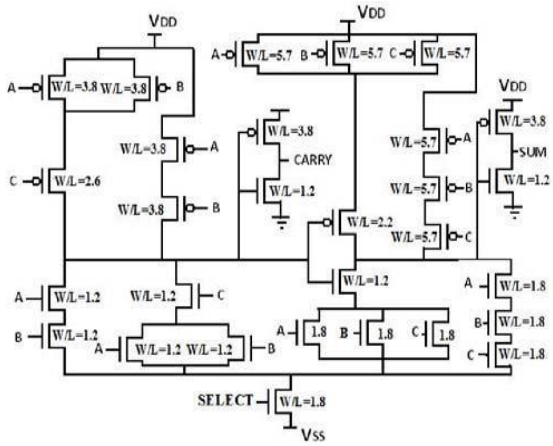

Figure 2**.** Proposed full adder (Design1) circuit with sleep s shown

Sleep transistor method has many disadvantages due fast raising of transistor from sleep to active mode it produces much power dissipation at a time which leads to Peak ground bounce noise affect for this reduction many modulation techniques are proposed for sleep signal 1.Single phase sleep signal slew rate modulation technique

2. Triple phase modulation 3. Step wise Vgs technique. These technique which in turn having disadvantages of occupying more space which leads to hike in power consumption as well power dissipation.

So, in this paper we proposing a new technique called dual stack technique to reduces more power.

Dual Stack Technique

Another technique for leak power reduction is that the stack approach, that forces a stack impact by breaking down associate degree existing semiconductor unit into 2 0.5 Size transistors [7]. The divided transistorNMOS1ncrease delay considerably and will limit the quality of the approach. The sleepy-eyed stack approach (Fig. 2) combines the sleep and stack approaches [2, 3]. The sleepy-eyed stack

technique divides existing semiconductor unit NMOS1nto 2 0.5 Size transistors just like the stack approach. Then sleep transistors square measure additional in parallel to 1 of the divided transistors. Throughout sleep mode, sleep transistors square measure turned off and stacked transistors suppress leak current whereas saving state. Every sleep semiconductor unit, placed in parallel to the one in all the stacked transistors, reduces resistance of the trail, therefore delay is diminished throughout active mode. However, space penalty may be a NMOS1gnificant matter for this approach NMOS1nce each semiconductor unit is replaced by 3 transistors and NMOS1nce further wires square measure additional for S and S', that square measure sleep Signals. Another technique known as twin sleep approach [8] (Fig. 3) uses the advantage of exploitation {the 2|the 2} additional pull- up and two additional pull-down transistorNMOS1n sleep mode either in OFF state or in ON state. NMOS1nce the twin sleep portion may be created common to any or all logic electronic equipment, less variety of transistorNMOS1s required to use a precise logic circuit.

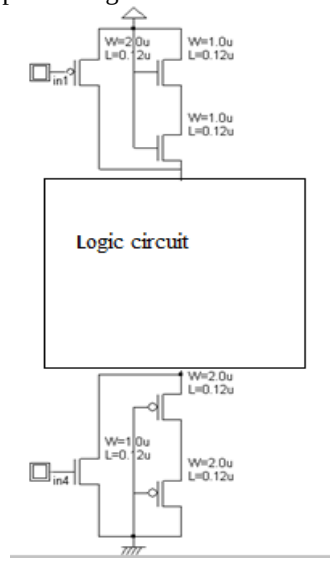

Fig3: Dual Stack Approach

III.SIMULATION ENVIRONMENT

The Methodology consists of 3 Modules.

- Logic circuit design, simulation, and Verilog file generation using DSCH.
- Layout design using MICROWIND.
- Simulation.

Here the traditional technique corresponds to SCEER flip-flop while not exploitation twin Stack approach. Within the analysis this circuit is mentioned as Base Circuit. And the changed technique corresponds to SCCER exploitation twin Stack Approach and mentioned within the analysis. The planned style i.e. Novel twin stack approach uses zero.12µm technology and operated with one.2V provide voltage The simulation parameter s are analyzed with the assistance of the Micro wind tool (version 2) and DSCH (version 2) for the schematic verification.

DSCH (Digital Schematic)

The DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex logic structures

DSCH also features the symbols, models and assembly support for 8051 and 16F84 controllers. The highlights are:-

- Supports Hierarchical logic design.
- Generates a Verilog description of the schematic for layout conversion.
- Immediate access to symbol properties (Delay & Fan-out)
- Model and assembly support for 8051 and PIC 16F84 Microcontrollers.

Sub-Micron, deep-submicron and Nano scale technology support

Micro wind

The Micro wind may be a tool for planning and simulating circuits at layout level. The tool options full written material facilities (copy, cut, past, duplicate, move), varied views (MOS characteristics, 2nd cross section, 3D method viewer), and an analog machine. The Micro wind program permits planning and simulating an microcircuit at physical description level. The package contains a library of common logic and analog ICs to look at and simulate. The Micro wind includes all the commands for a mask editor also as original tools ne'er gathered before in an exceedingly single module (2D and 3D method read, Verilog compiler, tutorial on MOS devices). you'll be able to gain access to Circuit Simulation by pressing one single key. the electrical extraction of your circuit is mechanically performed and therefore the analog machine produces voltage and current curves straight off.

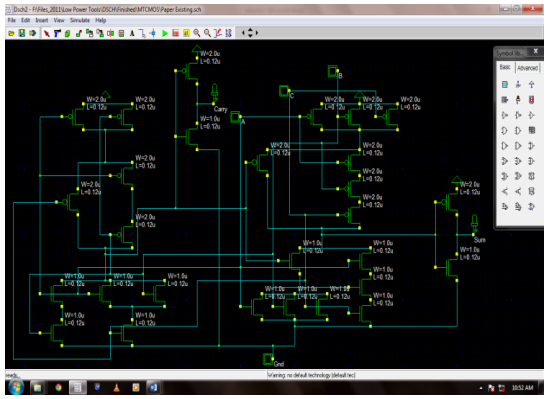

Fig 4: DSCH design of full adder

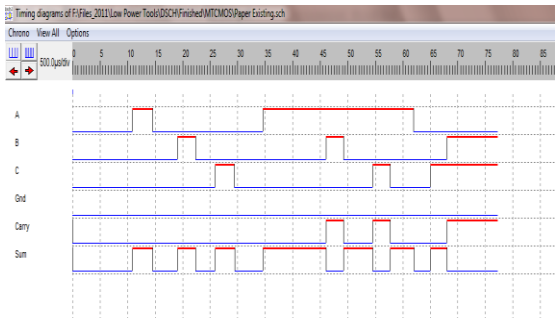

Fig 5: simulation wave form of fulladdercircuit

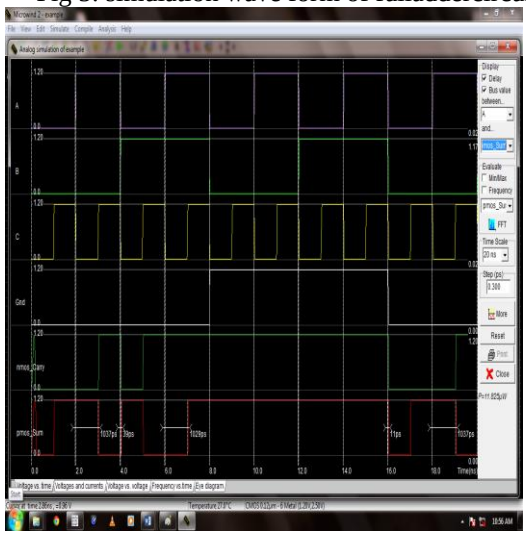

Fig 6: power dissipation an Export Micro wind

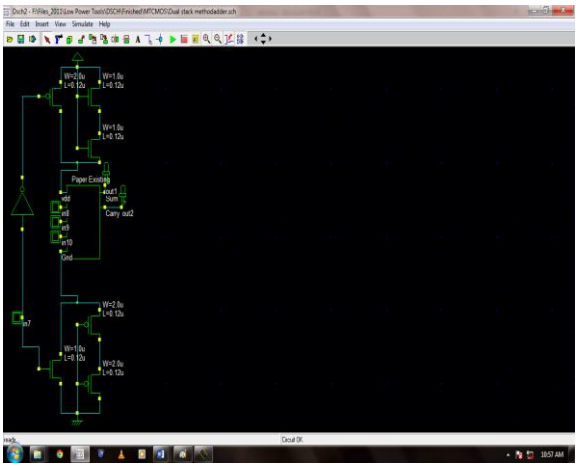

Fig 7: DSCH design of Dual stack Full adder

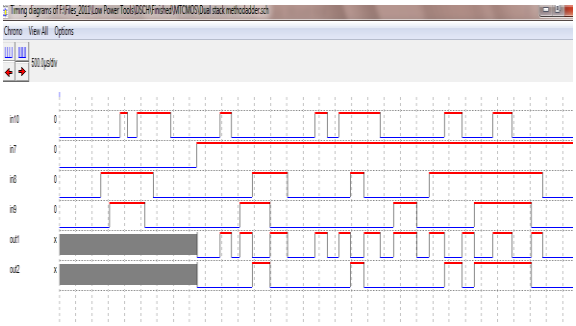

Fig 8: Simulation wave form of Dual stack full adder

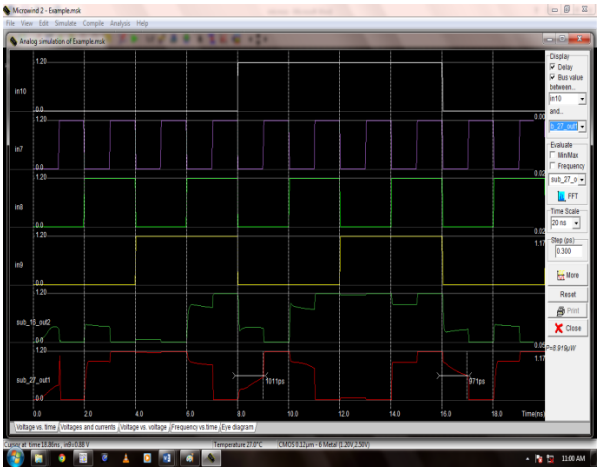

Fig 9: power dissipation an export micro wind

IV.Conclusion:

In nm scale CMOS technology, sub -threshold outpouring power consumption could be a nice

challenge. though previous approaches square measure effective in some ways in which, no good resolution for reducing outpouring power consumption is however far-famed. Therefore, designers select techniques based mostly upon technology and style criteria. During this paper, we offer novel circuit structure named "Dual stack" as a brand new remedy for designers in terms of static power and dynamic powers. In contrast to the sleep semiconductor technique, the Dual stack technique retains the first state. The Dual stack approach shows the smallest amount power dissipation among all strategies.

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