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DESIGN OF LOW POWER FULL ADDER USING POWER GATING SCHEME

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ABSTRACT:

Static power consumption could be a major concern in metric linear unit technologies. Beside technology reducing and better operational speeds of CMOS VLSI circuits, the discharge power is obtaining increased. As method geometries are getting smaller, device density will increase and threshold voltage additionally as compound thickness decrease to stay pace with performance we are using many types of power gating techniques. In this paper we are going to analyze the CMOS full adder using different types of power gated circuits using low power VLSI design techniques and we are going to display the comparison results between different nanometer technologies. The NMOS simulations were done using Micro wind Layou Editor & DSCH software and the results were given below.

Keywords: CMOS, VLSI, Power Gating,

1. INTRODUCTION:

The scaling of process technologies to nanometer regime has resulted in a rapid increase in leakage power dissipation NMOS. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity. The power reduction must be achieved without trading-off performance which makeNMOS it harder to reduce leakage during normal (runtime) operation.

On the other hand, there are several techniques for reducing leakage power in *sleep* or *standby* mode. Power gating is one such well known technique where a *sleep transistor* is added between actual ground rail and circuit ground (called *virtual ground*). This device is turned-off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a

substantial reductionin leakage at a minimal impact on performance

With reducing channel length for consecutive technology generations, threshold voltage AND circuit chemical compound thickness are being scaled down. Outflow current consequently will increase exponentially with reduction in threshold voltage. As per the ITRS [1], outflow current goes to be a limiting issue for consecutive lowering of transistors. Because of the smaller feature sizes in nm technologies, shorter channel lengths cause sub threshold current to extend once the semiconductor unit is within the off state. The lower sub threshold voltage offers rise to accrued sub threshold current furthermore, as a result of transistors can't be shifted fully.Since with each consecutive technology the quantity of transistors per given space is on an increase, the outflow power in associate microcircuit for consecutive generations is increasing, as a result of transistors leak even once they don't seem to be activated and important power dissipation takes place even throughout inactive state of circuits.

Power gating technique uses high Vt sleep transistors which cut off VDD from a circuit block when the block is not switching. The sleep transistor NMOS sizing is an important design parameter. This technique, also known as MTCMOS, or Multi-Threshold CMOS reduces stand-by or leakage power, and also enable NMOS Iddq testing.

Thus it's essential to scale back static power throughout the idle or standby mode of operation of the circuits. Full Adder area unit integral and very important parts of just about all processors, SOCs and Embedded Systems and area unit occupying a bigger space on chips. varied outpouring power reduction strategies area unit invariably applied to Full Adders to avoid wasting valuable battery resources in hand-held mobile applications. Since Full Adder peripheral circuits like input drivers, word line drivers, and output drivers occupy major portion of on chip caches in processors, savings in outpouring power of peripheral circuits is additionally advantageous for higher performance. Since the on chip memory use would possibly involve long inactivity states throughout cache misses or may be defrayment larger time in idle or sleep modes in some applications, static power reduction goes to be a bigger concern for such cases.

The dynamic (switching) power (P_D) and leakage power (P_{LEAK}) are expressed as

$$P_D = \alpha f C V_{DD}^2 \quad \ldots\ldots\ldots\ldots \quad (1)$$

$$P_{LEAK} = I_{LEAK} V_{DD} \quad \ldots\ldots\ldots\ldots \quad (2)$$

where α is the switching activity; f is the operation frequency, C is the load capacitance, VDD is the supply voltage and I_{LEAK} is the cumulative leakage current due to all the components of the leakage current.

Power gating affects style design quite clock gating. It will increase time delays as power gated modes got to be safely entered and exited. discipline trade-offs exist between coming up with for the quantity of run power saving in low power modes and therefore the energy dissipation NMOS to enter and exit the low power modes. motility down the blocks is accomplished either by software system or hardware. Driver software system will schedule the facility

down operations. Hardware timers is utilised. a frenzied power management controller is an alternative choice.

An outwardly switched power offer could be a terribly basic NMOS sort of power gating to attain future run power reduction. To shut off the block for little intervals of your time, internal power gating is a lot of appropriate. CMOS switches that give power to the electronic equipment ar controlled by power gating controllers. Outputs of the facility gated block discharge slowly. therefore output voltage levels pay longer in threshold voltage level. this could result in larger tangency current.

Power gatinguses low-leakage PMOS transistors as header switches to shut off power provides to components of a style in standby or sleep mode. NMOS footer switches may be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the facility offer and a virtual power network that drives the cells and may be turned off.

The quality of this complicated power network is important to the success of a power-gating style.2of the foremost important parameters ar the IR-drop and therefore the penalties NMOS. In NMOS chemical element space and routing resources. Power gating is enforced exploitation cell- or cluster-based (or fine grain) approaches or a distributed coarse grained approach.

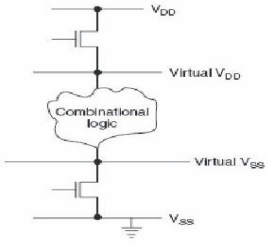


Fig1: Power Gated Circuits

II.Power-gating parameters

Power gating implementation has extra concerns NMOS for temporal arrangement closure implementation. the subsequent parameters got to be thought-about NMOS and their values rigorously chosen for a victorious implementation of this technique.

1. Power gate Size: the ability gate Size should be elite to handle the quantity of switch current at any given time. The gate should be larger specified there's no measurable voltage (IR) drop as a result of the gate. As a rule of thumb, the gate Size is chosen to be around three times the switch capacitance. Designers can even choose from header (P-MOS) or footer (N-MOS) gate. sometimes footer gates tend to be smaller in space for constant switch current. Dynamic power analysis NMOS tools will accurately live the switch current and conjointly predict the scale for the ability gate.

2. Gate management slew rate: In power gating, this NMOS a vital parameter that determines the ability gating potency. once the slew rate is massive, it takes longer to modify off and switch-on the circuit and thence will have an effect on the ability gating potency. Slew rate is managementled through buffering the gate control Signal.

3. NMOS concurrent switch capacitance: This NMOS vital constraint refers to the quantity of circuit that may be switched NMOS at the same time while not touching the ability network integrity. If an outsized quantity of the circuit is switched NMOS at the same time, the ensuing "rush current" will compromise the ability

network integrity. The circuit has to be switched in stage NMOS so as to stop this.

4. Power gate leakage: NMOS since power gates ar fabricated from active transistors, outflow reduction is a vital thought NMOS to maximise power savings.

i) Fine-grain power gating

Adding a sleep junction transistor to each cell that's to be turned off imposes an outsized space penalty, and singly gating the ability of each cluster of cells creates temporal arrangement issue NMOS introduced by inter-cluster voltage variation that ar tough to resolve. Fine-grain power gating encapsulates the switch junction transistor as a vicinity of the quality cell logic. switch transistors ar designed by either the library scientific discipline trafficker or voltaic cell designer. sometimes these cell styles adapt to the traditional voltaic cell rules and might simply NMOS be handled by EDA tools for implementation.

The Size of the gate management is meant considering NMOS the worst case situation which will need the circuit to modify throughout each clock cycle, leading to an enormous space impact. a number of the recent style NMOS implement the fine-grain power gating by selection, however just for the low Green Mountain State cells. If the technology permits multiple Green Mountain State libraries, the utilization of low Green Mountain State device NMOS is minimum within the style (20%), so the world impact is reduced. once victimisation power gates on the low Green Mountain State cells the output should be isolated if consequent stage could be a high Green Mountain State cell. Otherwise it will cause the neighboring high Green Mountain State cell to possess outflow once output goes to Associate in Nursing unknown state as a result of power gating.

Gate management slew rate constraint is achieved by having a buffer distribution tree for the management Signals. The buffers should be chosen from a collection of continuously on buffers (buffers while not the gate management Signal) designed with high Green Mountain State cells. The inherent distinction between once a cell switches off with reference to another, minimizes the frenzy current throughout switch-on and switch-off.

Usually the gating junction transistor is meant as a high Green Mountain State device. Coarse-grain power gating offers more flexibility by optimizing the ability gating cells wherever there's low switch activity. outflowoptimisation needs to be done at the coarse grain level, swapping the low outflow cell for the high outflow one. Fine-grain power gating is a chic methodology leading to up to ten times outflow reduction. this kind of power reduction build NMOS it Associate in Nursing appealing technique if the ability reduction demand isn't glad by multiple Green Mountain State optimisation alone.

ii) Coarse-grain power gating

The coarse-grained approach implements the grid vogue sleep transistors that drives cells regionally through shared virtual power networks. This approach is a smaller amount sensitive NMOS to PVT variation, introduces less NMOS IR-drop variation, and imposes a smaller space overhead than the cell- or cluster-based implementations. In coarse-grain power gating, the ability-gating junction transistor could be aa part of the power distribution network instead of the

quality cell.There are two ways of implementing a coarse-grain structure:

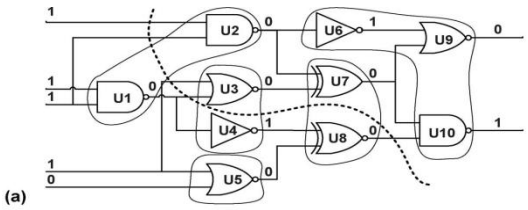


Fig2: Device without Power gating

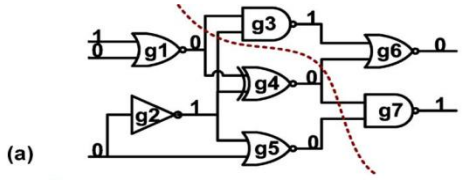


Fig3: Device with Power gating with reduced area & Power using clustering network formation

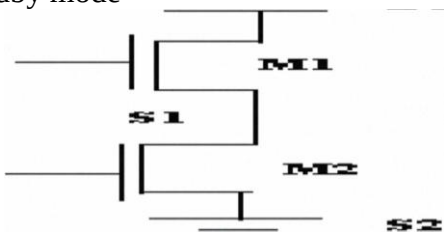
This work presented a logic clustering based solution to the problem of controlling/optimizing the power gating parameters. The key design considerationNMOS in the power mode transitions are minimizing the wakeup delay, the peak current, and the total Size of sleep transistors. This work analyzed the relations between the three parameters, and solved the problem of finding logic clusters and their wakeup schedule that minimize the wakeup delay while satisfying the peak current and performance loss constraints.

A)Stacking power gating scheme:

Stacking power gating scheme works on two strategies
1 Reduction of leakage current by stacking effect

2. Reduction of ground bounce noise by controlling the intermediate node Voltage.

I. Strategy to reduce leakage current in standby mode



J.

By taking the advantage of stacking structure escape current may be controlled in standby mode. Here sleep transistors M one and M2 ar stacked. once in standby mode i.e. once M one and M2 each ar off. during this structure foremost, the escape current is reduced by stacking result, turning each M one and M2 sleep transistors OFF. This raises the intermediate node voltage VGN to positive values to tiny drain current. within the analyzed theme, the escape current is reduced by the stacking result, turning each mil and M2 sleep transistors OFF. This raises the intermediate node voltage VGND2 to positive values thanks to tiny drain current. Positive potential at the intermediate node has four effects:

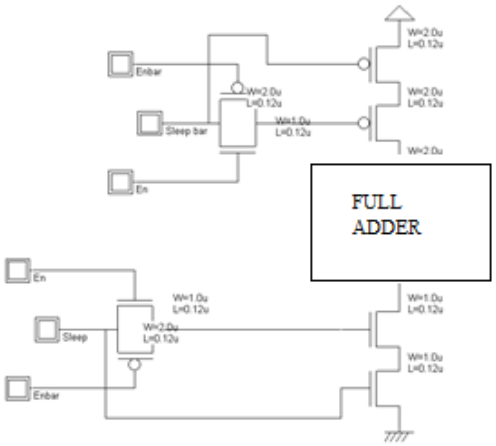
1)Gate to supply voltage of M I (Vgs I) becomes negative

2)Negative body• to• supply potential (Vbs I) of M I causes additional body result

3)Drain• to• supply potential (Vdsl) of money supply decreases, leading to less drain iatrogenic barrier lowering

4)Drain• to• supply potential (Vds2) of M2 is a smaller amount compared to money supply, as a result of most of the voltage drops across the money supply in sleep mode. This considerably reduces the drain iatrogenic barrier lowering.

III. **Proposed Power Gating based Sleep Technique**



The Above mentioned Sleep Circuit has three modes of operations

I. Active mode
2. Standby mode
3. Sleep to active mode transition

In active mode, the sleep Signal of the transistor is held at logic' 1 ' and both the sleep transistors M I and M2 (En and EnBar Transistors from the bottom side) remain ON. In this case both transistors offer very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply voltage.

There are several benefits of combining stacked sleep transistors. First the magnitude of power supply fluctuations sleep mode during mode transitions will be reduced because these transitions are gradual. Second, while conventional power gating uses a high- threshold device as a sleep transistor to minimize leakage, a stacked sleep structures can achieve the same effect with a normal threshold device

In active mode, the sleep Signal of the transistor is held at logic' 1 ' and both the sleep transistors NMOS1 and NMOS2 (NMOS Transistors used for sleep Purpose from the Bottom of the circuit) remain ON and control transistor is OFF by giving logic O. In this case both transistors offer very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply Voltage. And leakage current is reduced by the stacking effect, turning both NMOS1 and NMOS2 sleep transistors OFF. And vice versa for the header switch.

Positive potential at the intermediate node has four effects:

- Gate to source voltage of NMOS1 (VgsNMOS1) becomes negative.
- -Negative body -to-source potential (Vdsl) of NMOS1 decreases, resulting in less drain induced barrier lowering.
- Drain-to-source potential (VdNMOS2) of NMOS2 is less compared to NMOS1, because most of the voltage drops across the NMOS1 in sleep mode.

This significantly reduces the drain barrier lowering. The analyzed design gives major contribution in sleep to active mode in terms of peak of sleep mode compared to stacking power gating. Sleep mode occurs when circuit is going from sleep to active and vice versa. In first stage sleep transistor (NMOS1) working as diode by turn on the control transistor M I which is connected across the drain and gate of the sleep transistor (NMOS1). Due to this drain to source current of the sleep transistor dropNMOS in a quadratic manner. This reduces the voltage fluctuation on the ground and power net and it also reduces the

circuit wakeup time. So in sleep to active transition mode, we are turning ON transistor NMOS1 initially after small duration of time NMOS2 will be turned ON to reduce the GBN. In second stage control transistor is off that sleep transistor works normally.

During sleep to active mode transition, transistor NMOS1 is turned ON and transistor NMOS2 is turned ON after a small duration of time (6T). The logic circuit isolated from the ground for a short duration as the transistor NMOS2 is turned OFF. During this duration, the GBN can be greatly reduced by controlling the intermediate node voltage VGND2 and operating the transistor NMOS2 in triode region.
The intermediate node (VGND2) voltage can by

Inserting proper amount of delay, that is less than the discharging time of the NMOS1 transistor. Proper selection of the capacitance C2. Leakage current is reduced by the stacking effect, turning both NMOS1 and NMOS2 sleep transistors OFF. This raises the intermediate node voltage VGND2 to positive values due to small drain current. Positive potential at the intermediate node has four effects:

Gate to source voltage of NMOS1 (VgNMOS1) becomes negative. Negative body- to- source potential (VbNMOS1) of NMOS1 causes more body effect Drain- to-source potential (Vdsl) of NMOS1 decreases, resulting in less drain induced barrier lowering.

Drain-to-source potential (VdNMOS2) of NMOS2 is less compared to NMOS1, because most of the voltage drops across the NMOS1 in sleep mode this Significantly reduces the drain induced barrier lowering.

Results

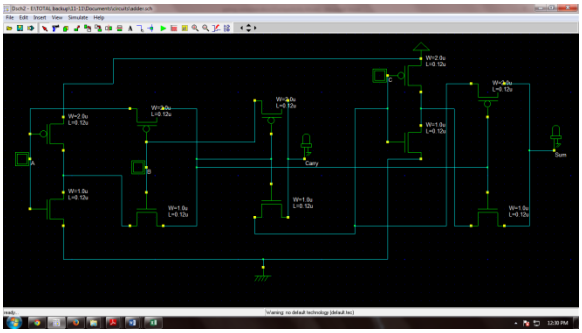


Fig : DSCH design of Full adder

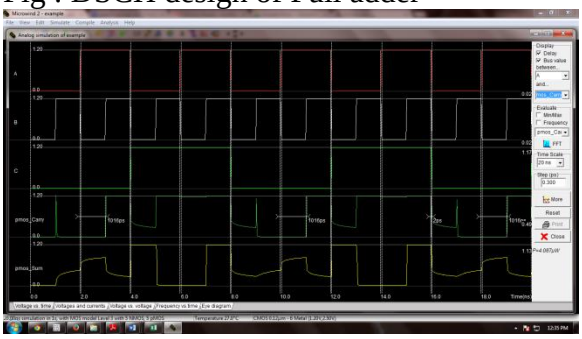


Fig : Micro wind Simulation of Full Adder

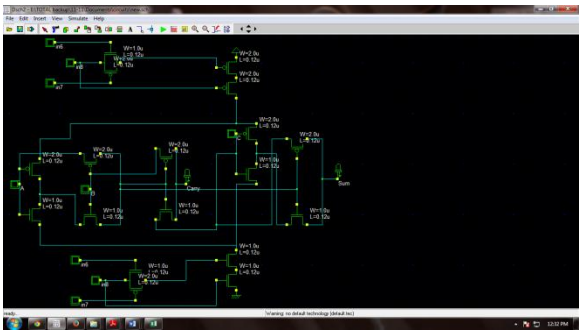


Fig: DSCH design of Proposed Power Gating

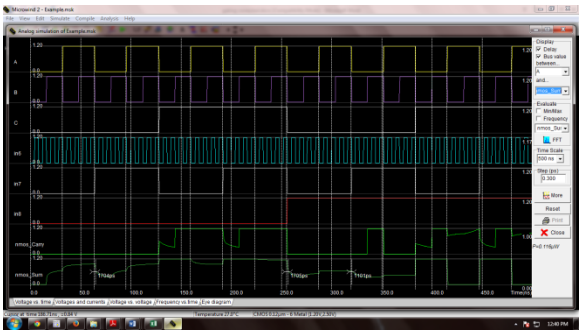


Fig: Micro wind Simulationof Proposed Power Gating

Tabulation:

Circuits	Area(um^2)	Power Dissipation
Full Adder	23*12	4.087uW
Full Adder with proposed Power Gating	40*15	0.116uW

V. Conclusion

In nanometer scale CMOS technology, sub threshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. In this paper, we provide novel circuit remedy for designer in terms of static power and dynamic powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product. Especially it shows nearly 50-60% of power than the existing normal or conventional flip-flops. So, it can be used for future integrated circuits for power & area Efficiency

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