



AN EFFECTIVE STRATEGY OF DESIGN ORIENTED LOW TRIGGERED POWER PULSE

Uttam Shahurao Munde¹, G.Deepthi², B.Sunilkumar³

¹M.Tech Student, Dept of ECE, Mannan Institute of Science & Technology, Chevella, R.R Dist,
A.P, India

²Assistant Professor, Dept of ECE, Mannan Institute of Science & Technology, Chevella, R.R Dist,
A.P, India

³Associate Professor, Dept of ECE, Mannan Institute of Science & Technology, Chevella, R.R Dist,
A.P, India

ABSTRACT:

In the design oriented strategy in which it is related to the aspect of the flip flop based triggering pulse in a well effective manner by the help of the low power well efficient strategy by which has been presented in the system in a well effective manner respectively. Initially the control logic based pulse generation based strategy takes place in a well effective manner followed by the gating function based on the logic operation of the AND in a well efficient phenomena where has been cancelled from the path related to the strategy of the critical phenomena in a well explicit manner by the help of the operation based on the rapid discharge oriented strategy in a well effective manner respectively. Here the system is designed with a well efficient framework oriented strategy in which it is related to the aspect of the reduced complexity based parameter by which in terms of the design oriented specification of the logic gated phenomena in a well effective manner followed by the strategy of the two transistor oriented strategy in a well effective manner respectively. In the next step factor there is an accurate analysis of the system with respect to the technique oriented with the enhancement of the pulse in a well effective manner followed by the conditional strategy where a design oriented path takes place in the system in a well efficient manner followed by the analysis of the rapid discharge in the system

in a well efficient manner followed by the analysis of the rapid discharge in the system based strategy in a well explicit manner respectively. Where by the implementation of the above design oriented strategy in a well efficient fashion there is a complete consumption of the power based strategy in a well efficient manner followed by the reduction of the pulse based on the triggered strategy and also the inverter based delay oriented phenomena followed by the well oriented aspect of the size of the transistor in a well effective manner respectively. Experiments have been conducted on the present method and huge number of analysis on the present design oriented strategy in which there is a improvement in the performance based scheme followed by the outcome in a well oriented fashion respectively.

Keywords: Triggered pulse circuit, FPGA (field programmable gate array), CPLD (complex programmable logic device), Flip flop respectively.

1. INTRODUCTION:

Here in the present strategy there is a major importance for the extensively utilization of the elements based on the strategy related to the aspect of the storage based phenomena in a well explicit manner with respect to the design oriented strategy of the digital logic based phenomena in a well efficient manner by the help of the flip flops in a well efficient manner respectively [1][2]. There is a lot of advancement in the technology related to the aspect of the design oriented strategy of the technique related to the aspect of the pipelining based phenomena in a well effective manner by the help of the simultaneous process of the multiple input in

an eager way that too in the well efficient fashion respectively [3][4]. Here in the present design oriented strategy in which there is a reduced power consumption based phenomena in a well effective manner followed by the regularization of the aspect related to the well efficient phenomena oriented with respect to the effective strategy of system oriented clock based consumption in a well explicit manner respectively.

BLOCK DIAGRAM

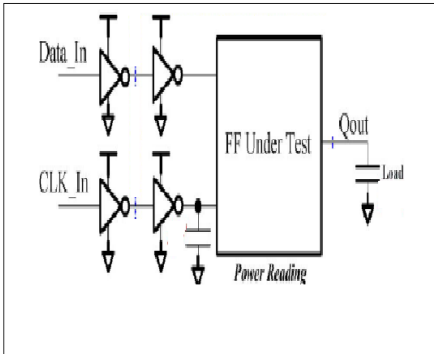


Fig1: shows the architectural representation of the present method respectively

2. METHODOLOGY

Here the present method completely overcome the drawbacks of the several previous methods in a well efficient manner [5][6]. In this paper a method is designed with a well effective framework oriented strategy in which there is an improvement in the performance followed by the outcome of the entire system in a well respective fashion [7][8]. Here the implementation aspect of the present method is shown in the above figure in the form of the block diagram and is explained in the elaborative fashion respectively[9][10]. There is a huge challenge for the present method where it is supposed to accurately analyze the problems of the several previous methods in a well

efficient manner and also used for the theoretical aspect oriented analysis in a representative fashion respectively. Here we finally conclude that the present design oriented mechanism is effective and efficient in terms of the improvement in the system based aspect respectively.

3. EXPECTED RESULTS

A comparative analysis is made between the present method to that of the several previous methods is shown in the below figure in the form of the graphical representation and explains in a brief elaborative fashion respectively. A lot of analysis is made on the present method and the huge number of the simulations have been conducted on the large number of the data sets in a well oriented fashion respectively. There is a huge challenge for the present method where it is supposed to improve the performance of the system followed by the overall system based analysis with respect to the outcome of the entire system respectively. Here we finally conclude that the present method is effective and efficient in terms of the performance based strategy in a well efficient manner respectively.

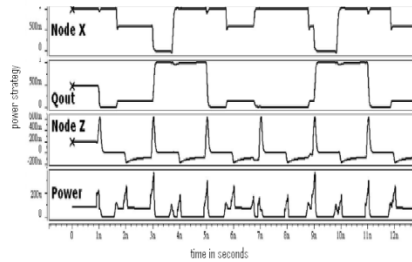


Fig 2: shows the graphical representation of the present method respectively

4. CONCLUSION

In this paper a method is designed with a well efficient framework oriented strategy in which it is one of the powerful technique for the effective implementation of the system in a well effective fashion respectively. Here a system is designed with a strategy of the FF triggered pulse oriented with the lower power strategy and a well effective device based phenomena for the analysis by the measure of the couple of the strategies in a well efficient manner respectively. Here the initial strategy is ana of the aspect of the stacked transistors is got reduced in the system based strategy in a well efficient manner followed by the path discharging with respect to the strategy of the AND logic oriented PTL incorporation strategy in a well efficient manner and the next one is related to the aspect of the

enhancement of the conditional strategy in a well explicit manner by the help of the pulse discharging related to the aspect of the width followed by the height in a well oriented fashion respectively. For the minimizing strategy of the pulse based reduction in a well effective fashion respectively. Here in the implementation of the proposed method oriented strategy there is an accurate evaluation of the system based strategy related to the aspect of the power followed by the delay based on the QQ in a well effective fashion respectively. Here we finally conclude that the present method is effective and efficient in terms of the outcome followed by the performance in a well efficient manner respectively.

REFERENCES

- [1] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R. Wang, A. Mehta, R. Heald, and G. Yee, "A newfamily of semi-dynamic and dynamic flip flops with embedded logic for high-performance processors," IEEE J.Solid-State Circuits, vol. 34, no. 5, pp. 712–716, May 1999.
- [2] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional precharge techniques for power-efficient dual-edge clocking," in Proc. Int. Symp. Low-Power Electron. Design, Monterey, CA, Aug. 12–14, 2002, pp. 56–59.

- [3] H. Partovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in IEEE Tech. Dig. ISSCC, 1996, pp. 138–139.
- [4] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," IEEE J. Solid-State Circuits, vol. 33, no. 5, pp. 807–811, May 1998.
- [5] C. K. Teh, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y. Oowaki, "Conditional data mapping flip-flops for low-power and high-performance systems," IEEE Trans. Very Large Scale Integr. (VLSI) Systems, vol. 14, pp. 1379–1383, Dec. 2006.
- [6] S. D. Naffziger, G. Colon-Bonet, T. Fischer, R. Riedlinger, T. J. Sullivan, and T. Grutkowski, "The implementation of the Itanium 2 microprocessor," IEEE J. Solid-State Circuits, vol. 37, no. 11, pp. 1448–1460, Nov. 2002.
- [7] A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel high speed sense-amplifier-based flip-flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 11, pp. 1266–1274, Nov. 2005.
- [8] P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and low power conditional discharge flip-flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 477–484, May 2004.
- [9] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," IEEE J. Solid-State Circuits, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.
- [10] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," in Proc. ISPLED, 2001, pp. 207–212.