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AN ANALYSIS OF GROUND BOUNCE NOISE REDUCTION IN FLIP-FLOP NETWORKS

M.Raghu[1], V.Sabitha[2]

[1]**M.Tech Student, Dept of ECE, Vaagdevi College of Engineering & Technology, Warangal, A.P, India**

raghu.masu@gmail.com

[2]**Asst Professor, Dept of ECE, Vaagdevi College of Engineering & Technology, Warangal, A.P, India**

sabithavem@gmail.com

ABSTRACT:

In this paper by using power gating technique we reduced the leakage power of the Conditional Data Mapping Flip-flop. In, this present days low power technology is increasing rapidly, majorly circuits was effected by the leakage power due various scaling techniques applied on the circuits to reduce the area occupancy of the circuit which in deed increases the power dissipation of the circuit. That leakage power was reduced using different power gating circuits. Here we simulate our circuits using DSCH and Micro wind.

Keywords: Conditional Data Mapping Flip-flop, leakage power, DSCH and Micro wind.

1. INTRODUCTION:

The scaling of method technologies to nano metre regime has resulted during a fast increase in outflow power dissipation. Hence, it's become extraordinarily vital to develop style techniques to scale back static power dissipation during times of inactivity. the ability reduction should be achieved while not trading-off performance that makes it more durable to scale back outflow throughout traditional (runtime) operation. On the opposite hand, there area unit many techniques for reducing outflow power in sleep or standby mode. Power gating is one such renowned technique wherever a sleep electronic transistor is side between actual

ground rail AND circuit ground (called virtual ground). This device is turned-off within the sleep mode to cut-off the outflow path. it's been shown that this system provides a considerable reduction in outflow at a least impact on performance Power gating technique uses high American state sleep transistors that interrupt VDD from a circuit block once the block isn't change. The sleep electronic transistor size is a crucial style parameter. This system, conjointly called MTCMOS or Multi-Threshold CMOS reduces stand-by or outflow power, and conjointly allows Idd testing. Power gating affects style design over clock gating. It will increase time delays as power gated modes ought to be safely entered and exited. Branch of knowledge trade-offs exist between planning for the quantity of discharge power saving in low power modes and also the energy dissipation to enter and exit the low power modes. Motility down the blocks is accomplished either by computer code or hardware. Driver computer code will schedule the ability down operations. Hardware timers is utilised an avid power management controller is another choice. An outwardly switched power offer may be a terribly basic kind of power gating to attain future discharge power reduction. To shut off the block for little intervals of your time, internal power gating is a lot of appropriate. CMOS switches that offer power to the electronic equipment area unit controlled by power gating controllers. Outputs of the ability gated block discharge slowly. Therefore output voltage levels pay longer in threshold voltage level. This may result in larger short current.

Power gating uses low-leakage PMOS transistors as header switches to shut off power provides to elements of a style in standby or sleep mode. NMOS footer switches can even be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the ability offer and a virtual power network that drives the cells and may be turned off.

The quality of this advanced power network is important to the success of a power-gating style. 2 of the foremost important parameters area unit the IR-drop and also the penalties in semiconductor space and routing resources. Power gating is enforced mistreatment cell- or cluster-based (or fine grain) approaches or Distributed coarse-grained approach.

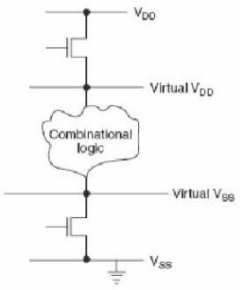

Fig1: Power Gated Circuits

II.Power-gating parameters

Power gating implementation has further issues for temporal order closure implementation. The subsequent parameters got to be thought-about and their values rigorously chosen for a productive implementation of this technique.

1. Power gate size: The facility gate size should be elect to handle the quantity of switch current at any given time. The gate should be larger such there's no measurable voltage (IR) drop attributable to the gate. As a rule of thumb, the gate size is chosen to be around three times the switch capacitance. Designers also can choose from header (P-MOS) or footer (N-MOS) gate. typically footer gates tend to be smaller in space for identical switch current. Dynamic power analysis tools will accurately live the switch current and conjointly predict the scale for the facility gate.

2. Gate management slew rate: In power gating, this can be a very important parameter that determines the facility gating potency. once the slew rate is giant, it takes longer to modify off and switch-on the circuit and thence will have an effect on the facility gating potency. Slew rate is management led through buffering the gate control signal.

3. Concurrent switch capacitance: This vital constraint refers to the quantity of circuit which will be switched at the same time while not touching the facility network integrity. If an outsized quantity of the circuit is switched at the same time, the ensuing "rush current" will compromise the facility network integrity. The circuit must be switched piecemeal so as to forestall this.

4. Power gate leakage: Since power gates are product of active transistors, leak reduction is a very important thought to maximise power savings.

i) Fine-grain power gating

Adding a sleep junction transistor to each cell that's to be turned off imposes an outsized space penalty, and one by one gating the facility of each cluster of cells creates temporal order problems introduced

by inter-cluster voltage variation that are tough to resolve. Fine-grain power gating encapsulates the switch junction transistor as a locality of the quality cell logic. Switch transistors are designed by either the library science merchant or voltaic cell designer. Typically these cell styles change to the conventional voltaic cell rules and may simply be handled by EDA tools for implementation. The size of the gate management is meant considering the worst case state of affairs which will need the circuit to modify throughout each clock cycle, leading to an enormous space impact. a number of the recent styles implement the fine-grain power gating by selection, however just for the low American state cells. If the technology permits multiple American state libraries, the employment of low American state devices is minimum within the style (20%), in order that the world impact may be reduced. once victimization power gates on the low American state cells the output should be isolated if successive stage may be a high American state cell. Otherwise it will cause the neighbouring high American state cell to possess leak once output goes to associate degree unknown state attributable to power gating. Gate management slew rate constraint is achieved by having a buffer distribution tree for the management signals. The buffers should be chosen from a group of perpetually on buffers (buffers while not the gate management signal) designed with high American state cells. The inherent distinction between once a cell switches off with reference to another, minimizes the frenzy current throughout switch-on and switch-off.

Usually the gating junction transistor is meant as a high American state device. Coarse-grain power gating offers additional flexibility by optimizing the facility gating cells wherever there's low switch activity. Leak optimisation must be done at the coarse grain level, swapping the low leak cell for the high leak one. Fine-grain power gating is a chic methodology leading to up to ten times leak reduction. This kind of power reduction makes it associate degree appealing technique if the facility reduction demand isn't glad by multiple American state optimisation alone

ii) Coarse-grain power gating

The coarse-grained approach implements the grid vogue sleep transistors that drive cells regionally through shared virtual power networks. This approach is a smaller amount

sensitive to PVT variation, introduces less IR-drop variation, and imposes a smaller space overhead than the cell- or cluster-based implementations. In coarse-grain power gating, the facility-gating semiconductor device could be a a part of the power distribution network instead of the quality cell. There are 2 ways that of implementing a coarse-grain structure:

1. Ring-based: the facility gates are placed round the perimeter of the module that's being switched-off as a hoop. Special corner cells are wont to flip the facility signals round the corners.

2. Column-based: the facility gates are inserted within the module with the cells abutted to every different within the variety of columns. The world power is that the higher layers of metal, whereas the switched power is within the lower layers.

Gate size depends on the general shift current of the module at any given time. Since solely a fraction of circuits switch at any purpose of your time, power gate sizes are smaller as compared to the fine-grain switches. Dynamic power simulation victimization worst case vectors will verify the worst case shift for the module and therefore the dimensions. The IR drop also can be factored into the analysis. Co-occurring shift capacitance could be a major thought in coarse-grain power gating implementation. so as to limit co-occurring shift, gate management buffers is flower bound, and special counters is wont to by selection activate blocks of switches.

III.Power Gating for Delay Reduction

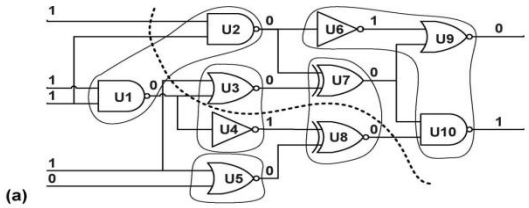

Fig2: Device without Power gating.

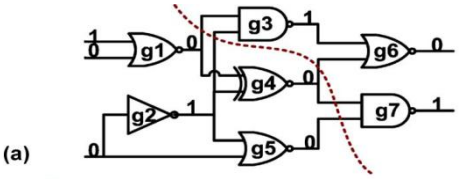

Fig3: Device with Power gating with reduced area & Power using clustering network formation.

This work presented a logic clustering based solution to the problem of controlling/optimizing the power gating parameters. The key design considerations in the power mode transitions are minimizing the wakeup delay, the peak current, and the total size of sleep

transistors. This work analyzed the relations between the three parameters, and solved the problem of finding logic clusters and their wakeup schedule that minimize the wakeup delay while satisfying the peak current and performance loss constraints major thought in coarse-grain power gating implementation. so as to limit co occurring shift, gate management buffers is flower bound, and special counters is wont to by selection activate blocks of switches.

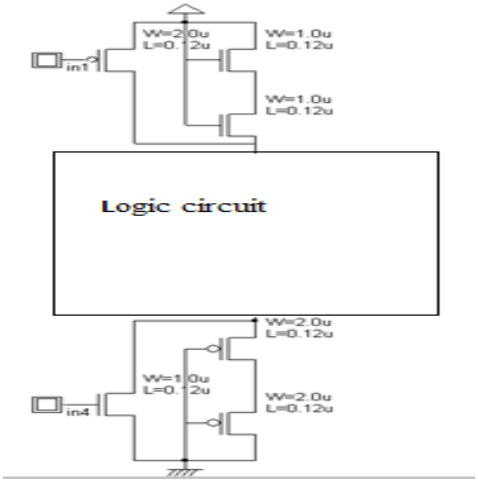

Fig4: Dual Stack Approach

A variation of the sleep approach, the zigzag approach, reduces wake- up overhead caused by sleep transistors by placement of alternating sleep transistors assuming a particular pre-selected input vector [6]. Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors [7]. The divided transistors increase delay significantly and could limit the usefulness of the approach. The sleepy stack approach (Fig. 2) combines the sleep and stack approaches [2, 3]. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach since every transistor is replacedby three transistors and since additional wires are added for S and S', which are sleep signals. Another technique called Dual sleep approach [8] (Fig. 3) uses the advantage of using the two extra pull- up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the dual sleep portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit.

The differences between these two power gating techniques are checked by designing a flip-flop's then simulated using the tools and snapshots are given below are given below. As flip-flops are most commonly used in all the digital circuits it is much needed to make the flip-flops much power efficient than all other devices. In this Part we are designing the low power flip-flops by reducing the power using power gated technology. The new flip-flop design's using Dual Stack method is shown below. The dual stack method has noise efficiency & power efficiency than normal flip-flops.

Conditional Data Mapping Flip-Flop

A new family of low-power and high-performance flip-flops, namely conditional data mapping flip-flops (CDMFFs), which reduce their dynamic power by mapping their inputs to a configuration that eliminates redundant internal transitions. We present two CDMFFs, having differential and single-ended structures, respectively, and compare them to the state-of-the-art flip-flops. The results indicate that both CDMFFs have the best power-delay product in their groups, respectively. In the aspect of power dissipation, the single-ended and differential CDMFFs consume the least power at data activity less than 50%, and are 31% and 26% less power than the conditional capture flip-flops at 25% data activity, respectively. In the aspect of performance, CDMFFs achieve small data-to-output delays, comparable to those of the transmission-gate pulsed latch and the modified-sense-amplifier flip-flop. In the aspect of timing reliability, CDMFFs have the best internal race immunity among pulse-triggered flip-flops. A post-layout case study is demonstrated with comparison to a transmission-gate flip-flop. The results indicate the single-ended CDMFF has 34% less in data-to-output delay and 28% less in power at 25% data activity, in spite of the 34% increase in size.

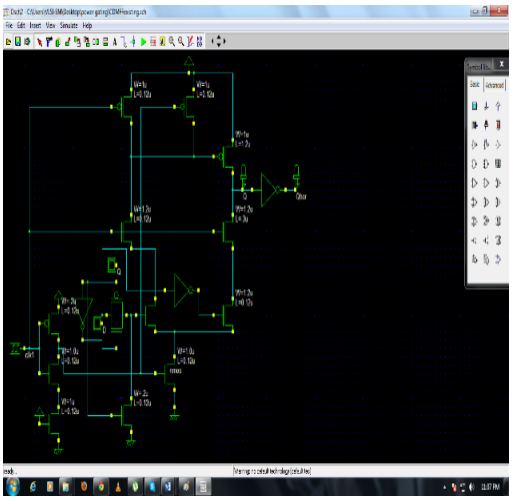

Fig5: Conventional CDMFF

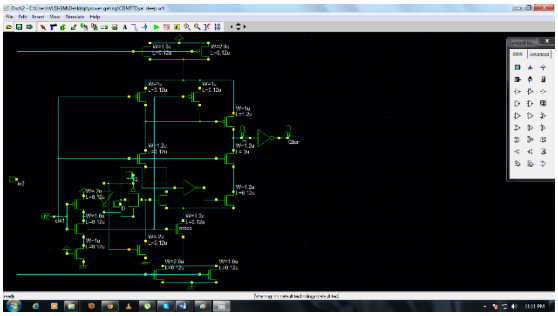

Fig 6: Conventional CDMFF Flip-flop using Power Gated Circuits using Dual sleep Technique

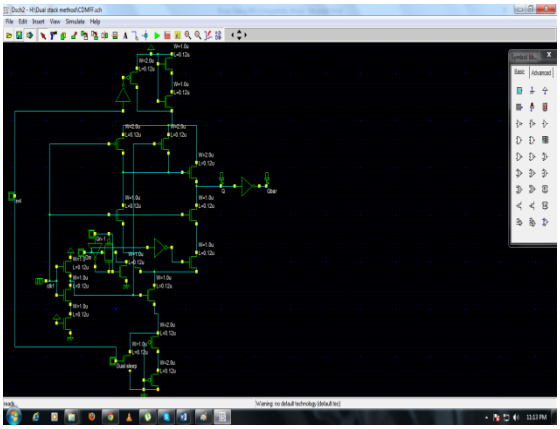

Fig 7: Conventional CDMFF Flip-flop using Power Gated Circuits with Dual stack approach

IV. Tabulation Results

Type	Area	Power
CDMFF	31um*13um	0.454mW
CDMFF with Dual Sleep	39um*15um	0.185mW
CDMFF with Dual Stack	44um*11um	0.355mW

Thus the Dual stack method shows much reduced power than all the circuits. But the area constraints have been considerably increased. But using scaling techniques we can improve the area constraints.

V. Conclusion

In nanometre scale CMOS technology, sub threshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. In this paper, we provide novel circuit structure named "Dual stack" as a new remedy for designers in terms of static power and dynamic powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product.

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