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# DESIGN AND SIMULATION OF MTCMOS CIRCUITS

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**ABSTRACT:**

Various high speed ordered multi-threshold voltage CMOS (MTCMOS) circuit techniques are conferred and evaluated during this paper. Ground bouncing noise made throughout the sleep to active mode transitions is a vital challenge in Multi-Threshold CMOS (MTCMOS) circuits. Various MTCMOS Circuits are evaluated using DSCH and Micro wind.

## 1. INTRODUCTION:

As the essential dimensions of MOSFETs still shrink, the availability voltage of integrated circuits is additionally scaled to keep up device dependability and to lower the speed of increase of the ability consumption. so as to keep up a satisfactory performance at a lower provide voltage, the edge voltage (Vth) of MOSFETs is additionally scaled. A lower threshold voltage but ends up in Associate in exponentially increase of sub threshold leakage current. The sub threshold leakage currents contribute considerably to the full power consumption of Associate in any microcircuit [1]. With the proliferation of moveable devices like cell phones and laptop computer computers with long idle periods, suppressing the subthreshold escape currents is extremely fascinating to increase the battery lifespan.

One of the popular escape power reduction ways applicable to idle circuits is MTCMOS [2]. In Associate in Nursing MTCMOS circuit, high threshold voltage (high -|V th|) sleep transistors (header and footer) area unit wont to bring to a halt the ability provide or the bottom affiliation to the idlelow threshold voltage (low-Vth) circuit blocks [3]. Once Associate in Nursing MTCMOS circuit transitions from the sleep mode to the active mode, high instant currents flow through the sleep transistors. massive voltage fluctuations occur on each the $64000 power cable (power bouncing noise) and also the real ground (ground bouncing noise)

MTCMOS circuit technique is widely adopted for enhanced energy efficiency in high-performance integrated circuits [1]-[9]. The MTCMOS technique suppresses the leakage currents by disconnecting the idle low threshold voltage (low-$|V_{th}|$) logic gates

from the power supply and/or the ground line via cut-off high threshold voltage (high-$|V_{th}|$) sleep transistors as shown in Fig 1.

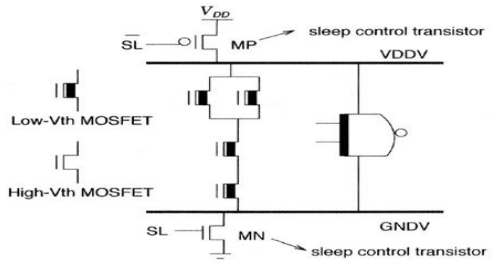


Fig1:MTCMOS technique applied to a logic circuit.

**Sleep Transistor Method:**

In sleep transistor method we are connecting an additional Nmos transistor at the ground network.Whenever circuit is in the static position then sleep transistor given input as zero.This makes grounddisconnect fromthe original circuit thereby reduces the leakage power.

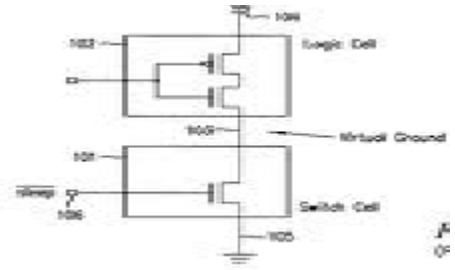

Fig 2: Sleep Transistor method

During the sleep to active mode of sleep transistor at a time leakage power will dissipates to ground which increase the ground bounce noise effect.To reduce this effect additional modulation circuits are added to sleep signal are illustrated below.

SINGLE-PHASE SLEEP SIGNAL SLEW RATE MODULATION

The effect of sleep signal raising from 0 to $V_{dd}$ level will increases the ground bounce noise effect on the circuit. So, the rise time delay of the sleep signal increased the time taken by the sleep transistor to reach saturation also increases which makes the decrease of ground bounce noise. When the sleep signal gradually rises from 0 V to $V_{DD}$ a When the voltage level of sleep signal is lower than the threshold voltage ($V_{th\_sleep}$) of sleep transistor, the sleep transistor operates in weak inversion region. The virtual ground line (VGND) is discharged very slowly by the small leakage current produced by the high-$|V_{th}|$ sleep transistor The noise induced on the ground distribution network is negligible for $^{V}gs<^{V}th\_sleep$.

After the sleep signal rises above the threshold voltage of sleep transistor, the VGND is discharged faster. Noise on the real ground is thereby increased. Subsequently, when the VGND is discharged to one threshold voltage (low-$V_{th\_nMOS}$) below the voltages of the internal nodes in the low-$|V_{th}|$ .circuit block, the parasitic capacitors of internal nodes start discharging as well. Another wave of bouncing noise is thereby produced on the real ground wires.

In SLEEP mode, VGND and all the internal nodes of low-$|V_{th}|$ circuit block are maintained at voltage levels close to $V_{DD}$. During a reactivation event, the internal nodes of the low-$|V_{th}|$ circuit block transition to the correct logic states stage by stage depending on the primary input vectors [7]. Some internal nodes follow the discharging VGND and transition toward 0 V. Significant amount of switching and short-circuit currents are produced by the awakening low-$|V_{th}|$ logic block.

The above three techniques Single phase Modulation, TPS, step-wise Vgs uses additional circuitry to the existing sleep

transistor which indeed increases the power consumption and also power dissipation. So, in this paper we are applying a new technique called dual stack technique applied to a SCCER Flip –flop network.

**Dual Stack Technique**

Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half Size transistors [7]. The divided transistorNMOS1ncrease delay significantly and could limit the usefulness of the approach. The sleepy stack approach (Fig. 2) combines the sleep and stack approaches [2, 3]. The sleepy stack technique divides existing transistor NMOS1nto two half Size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a NMOS1gnificant matter for this approach NMOS1nce every transistor is replaced by three transistors and NMOS1nce additional wires are added for S and S', which are sleep Signals. Another technique called Dual sleep approach [8] (Fig. 3) uses the advantage of using the two extra pull- up and two extra pull-down transistorNMOS1n sleep mode either in OFF state or in ON state. NMOS1nce the dual sleep portion can be made common to all logic circuitry, less number of transistorNMOS1s needed to apply a certain logic circuit.

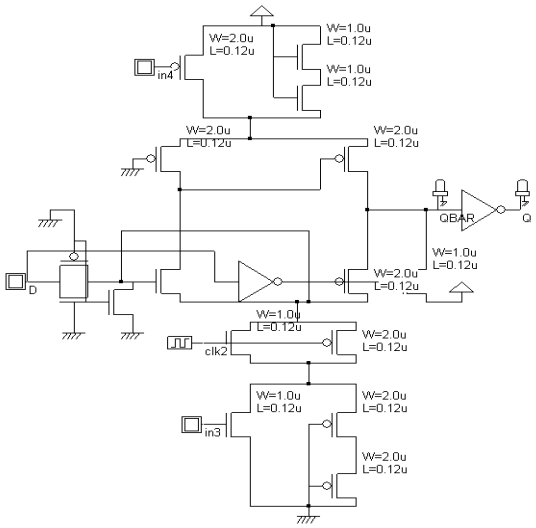


Fig 8: SCCER Flip-Flop using Power Gated Circuits

**SIMULATION ENVIRONMENT**

The Methodology consists of 3 Modules.

- Logic circuit design, simulation, and Verilog file generation using DSCH.
- Layout design using MICROWIND.
- Simulation.

Here the Conventional technique corresponds to SCEER filpflop without using Dual Stack approach. In the analysis this circuit is mentioned as Base Circuit.
And the Modified technique corresponds to SCCER using Dual Stack Approach and mentioned in the analysis. The proposed design i.e Novel dual stack approach uses 0.12µm technology and operated with 1.2V supply voltage

The simulation parameter s have been analyzed with the help of the Microwind tool (version 2) and DSCH (version 2) for the schematic verification.

**DSCH (Digital Schematic)**

The DSCH program is a logic editor and

simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex logic structures

DSCH also features the symbols, models and assembly support for 8051 and 16F84 controllers. The highlights are:-

- Supports Hierarchical logic design.
- Generates a Verilog description of the schematic for layout conversion.
- Immediate access to symbol properties (Delay & Fan-out)
- Model and assembly support for 8051 and PIC 16F84 Microcontrollers.

Sub-Micron, Deep – submicron and nanoscale technology support

**Microwind**

The Microwind is a tool for designing and simulating circuits at layout level. The tool features full editing facilities (copy, cut, past, duplicate, move), various views (MOS characteristics, 2D cross section, 3D process viewer), and an analog simulator. The Microwind program allows designing and simulating an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. The Microwind includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, Verilog compiler, tutorial on MOS devices). You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

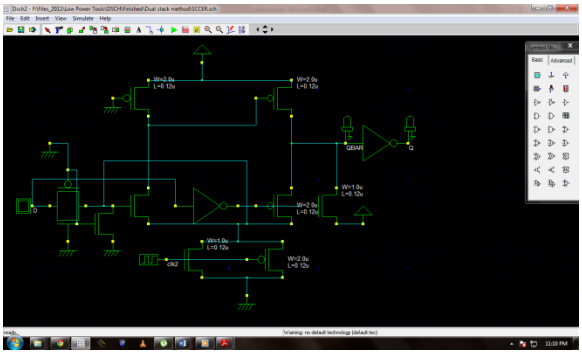

**Fig: DSCH design of SCCER Filp-Flop**

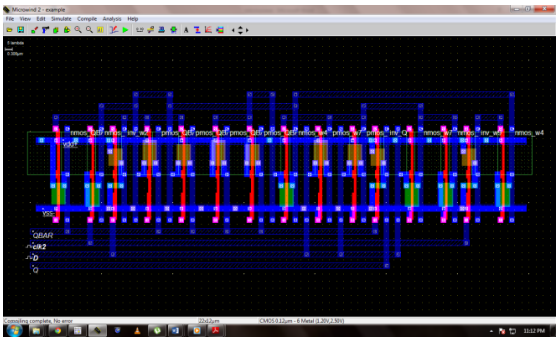

**Fig: Layout diagram**

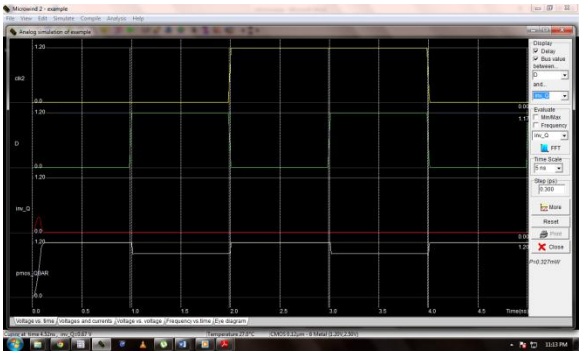

**Fig: Simulation Wave form in Micro wind**

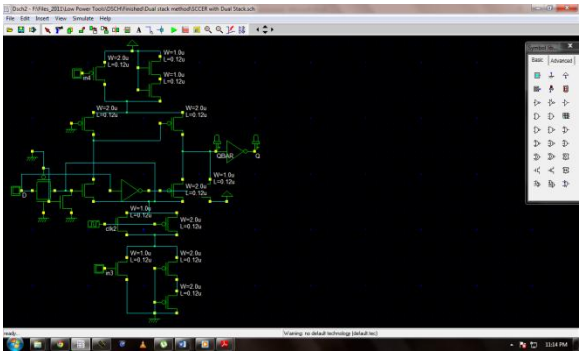

**Fig: : DSCH design of dual stack SCCER Flip-Flop**

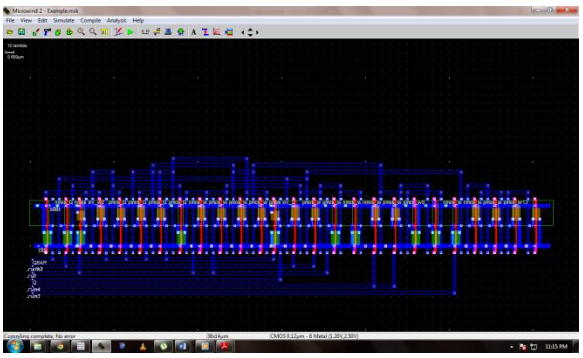

**Fig: Layout diagram**

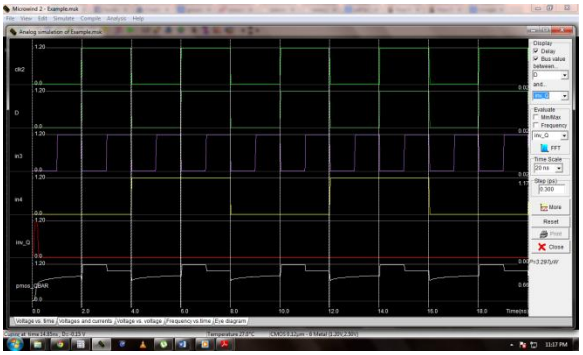

**Fig: Simulation waveforms in Micro wind**

**Tabulation of Results:**

| **Circuit** | **Area(um$^{2)}$** | **Power Dissipation** |
|---|---|---|
| SCCER | **22*12** | **0.327 mW** |
| SCCER With dual stack | **38*14** | **3.297uW** |

**Conclusion:**

In nanometer scale CMOS technology, sub - threshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. In this paper, we provide novel circuit structure named "Dual stack" as a new remedy for designers in terms of static power and dynamic powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption

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